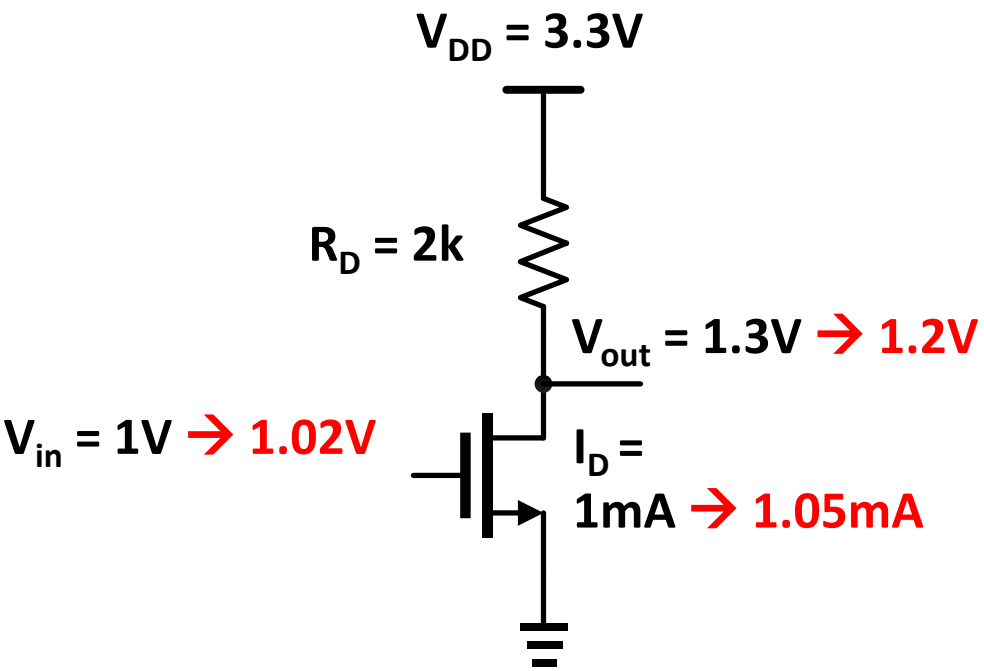
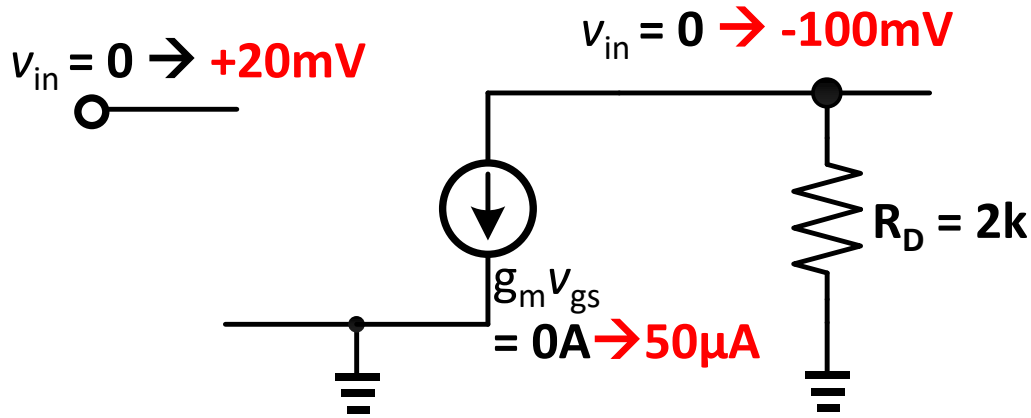
Common Source Amplifier (2)

Hanwool Jeong

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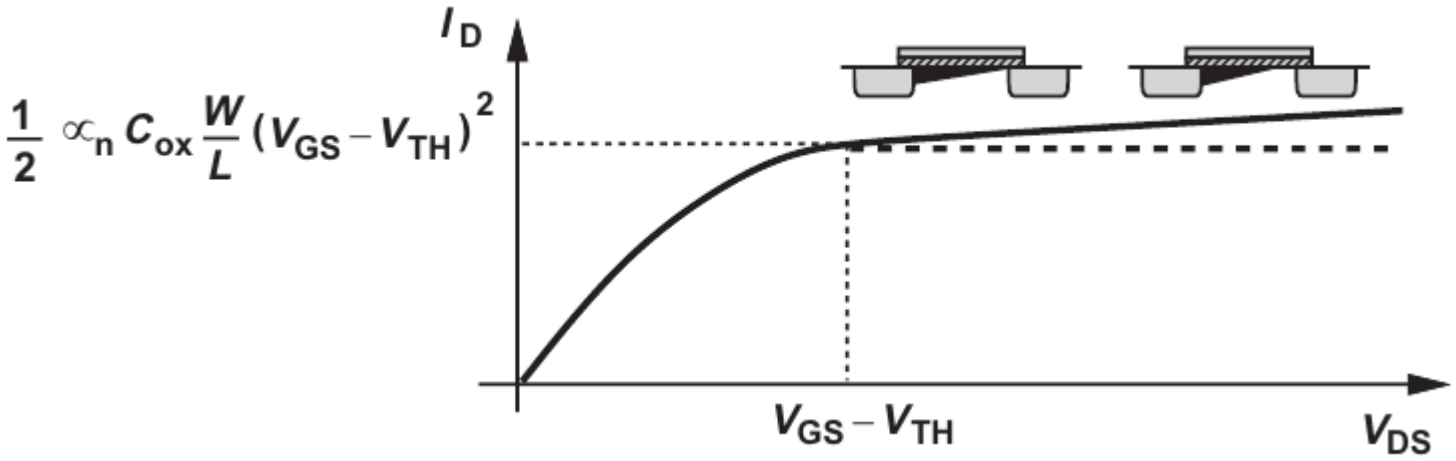
Small Signal Model vs. What Really Happens





Revisit Channel Length Modulation

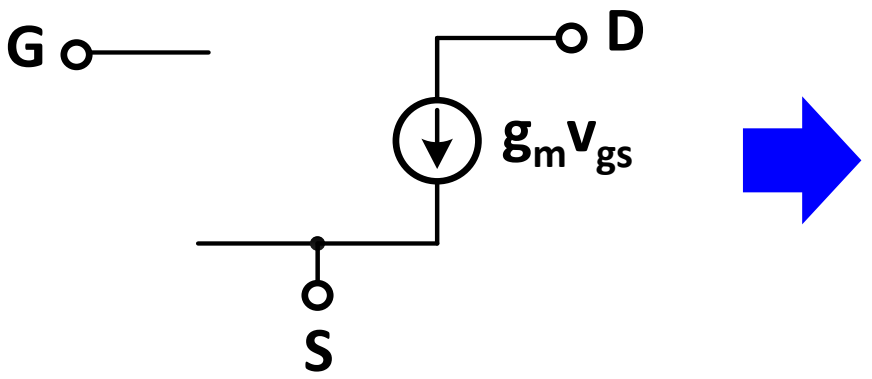
- You remember?
- Even in the saturation region, I_D is not completely independent to V_{DS}. Then what?



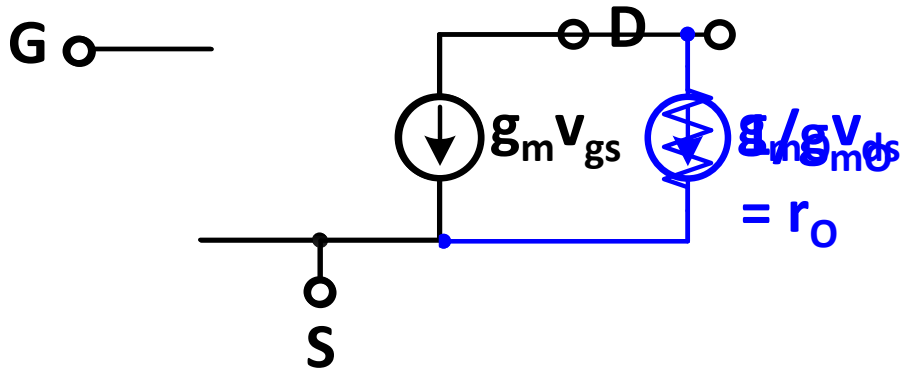
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

Small Signal Model w/ Channel Length Modulation

- PLEASE first predict it intuitively. Do not just accept it.
- It is
  - An additional current path
  - Dependent on V_{DS}



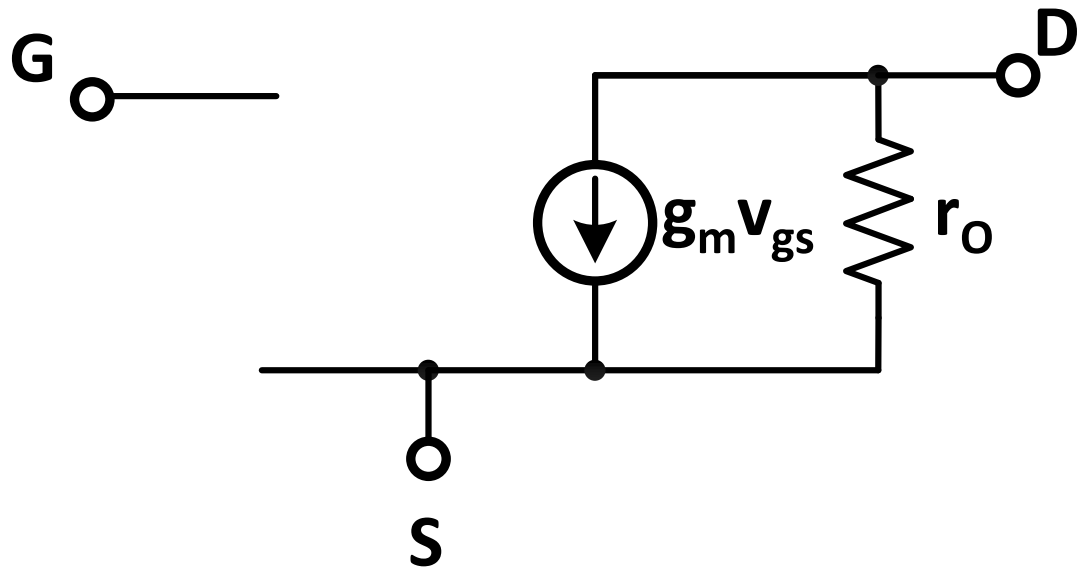
Channel length modulation X



Channel length modulation O

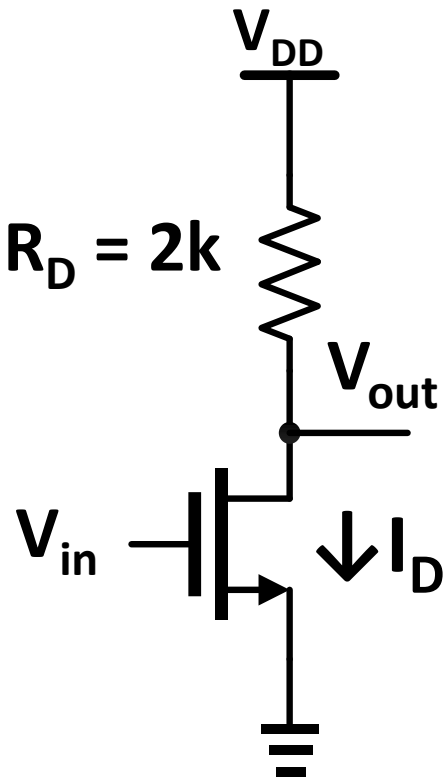
Small Signal Model w/ Channel Length Modulation

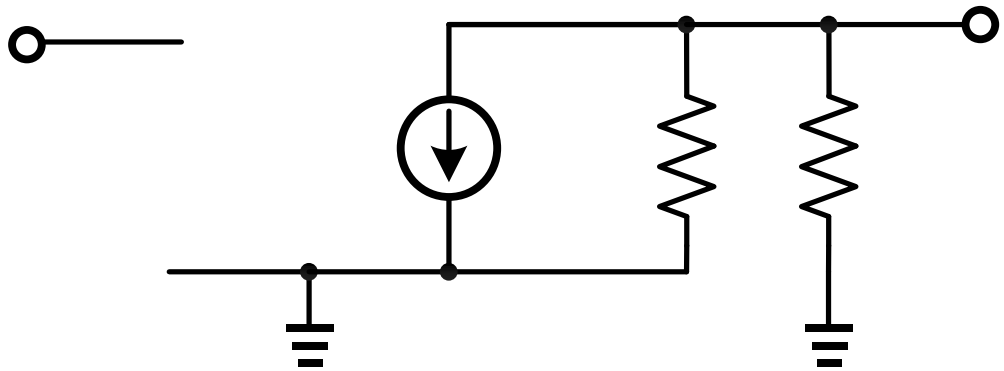
- Can you determine r_O from I-V model? Like you do in g_m.



CS Amplifier Gain When λ ≠ 0

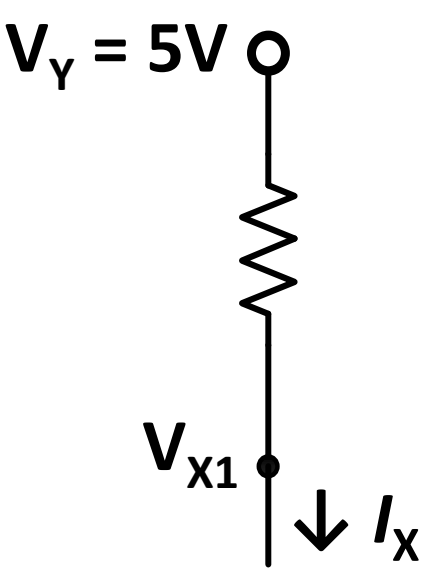
- Can you derive the gain? How is it changed?

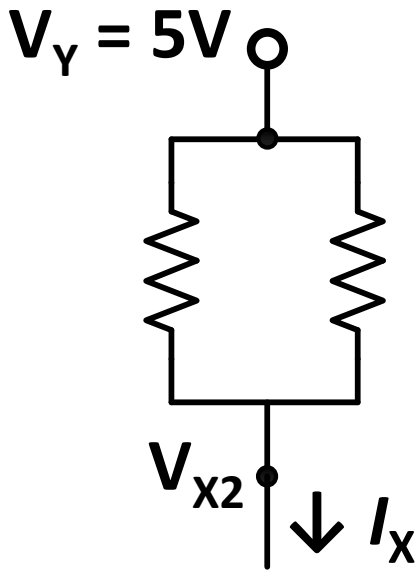




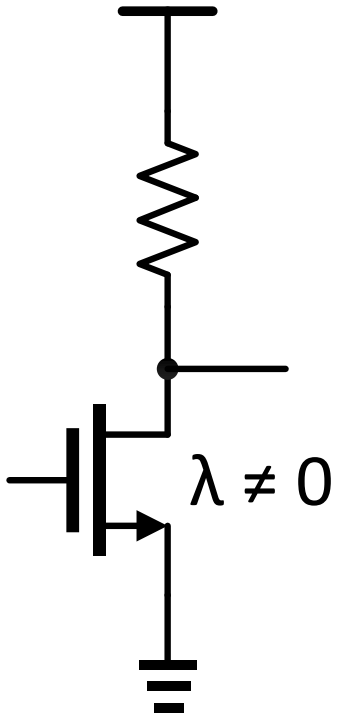
Impact of Path Addition

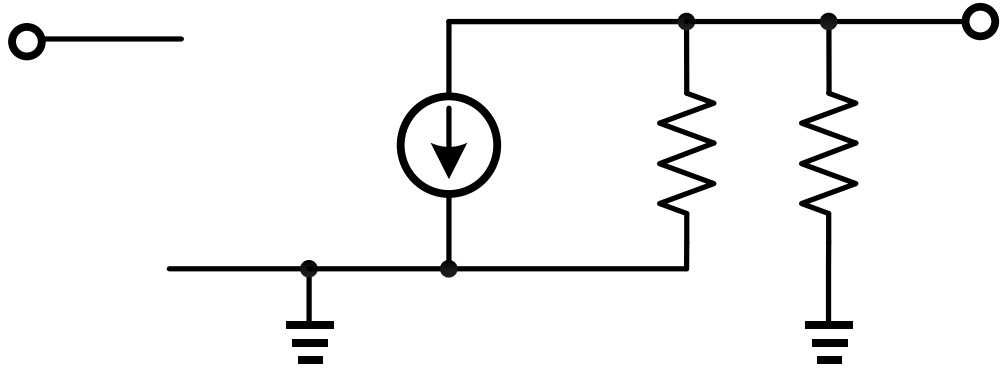
- How can you measure the effect of path adding?
- Mimic the same situation!





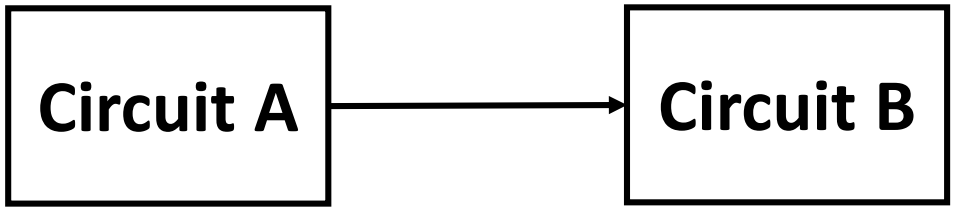
Can You Repeat “What Really Happens”





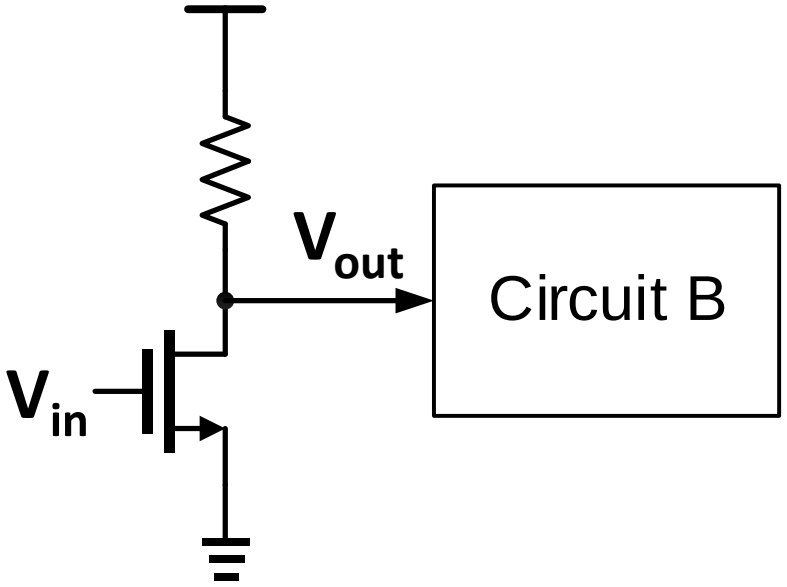
Amplifier Will be Connected with Other Circuits!

- Not only amplifier, but in any device, circuit, system, architecture accepting input and generating output,
- You should be aware of that
  - Input of current circuit is from the something else's output
  - Output of the current circuit will be connected to the something else's input
- Then, you should be questioning about:
  - **Is there any change or effect on output voltage according to the circuit which connected to the output node?**



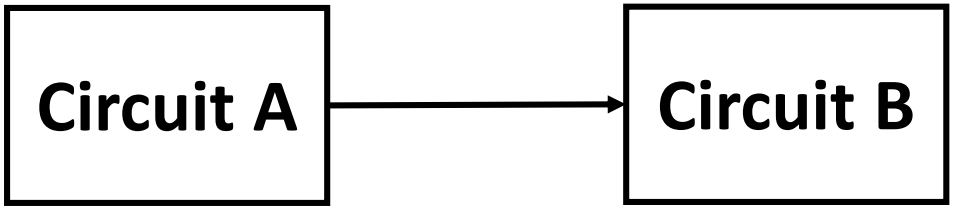
At Output Stage,

- How is it affected? Suppose that V_{in} is increased by small amount, which results in V_{out} decrease.
- We saw similar situation before!
  ➔ Path is added and output voltage magnitude is degraded.



In General,

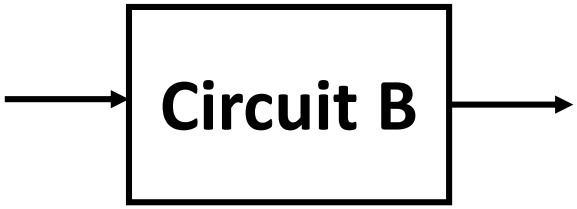
- When output is voltage, and input is voltage,



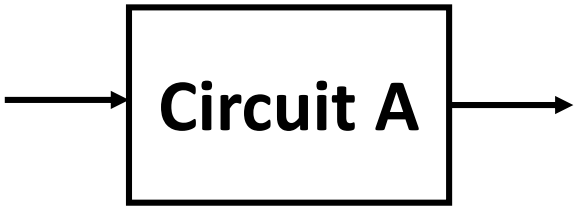
- Gain is changed by
- Or, effective voltage transfer ratio is changed by

Input Resistance and Output Resistance

- Input resistance, R_{in} is measured by

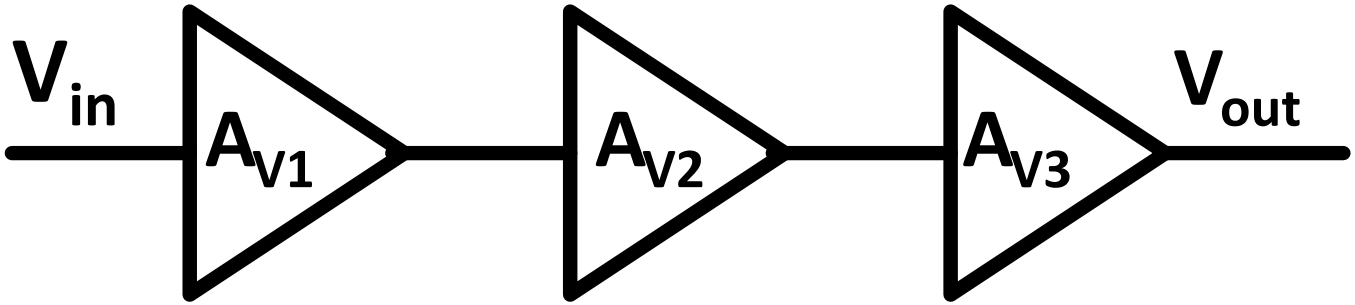


- Output resistance, R_{out} is measured by



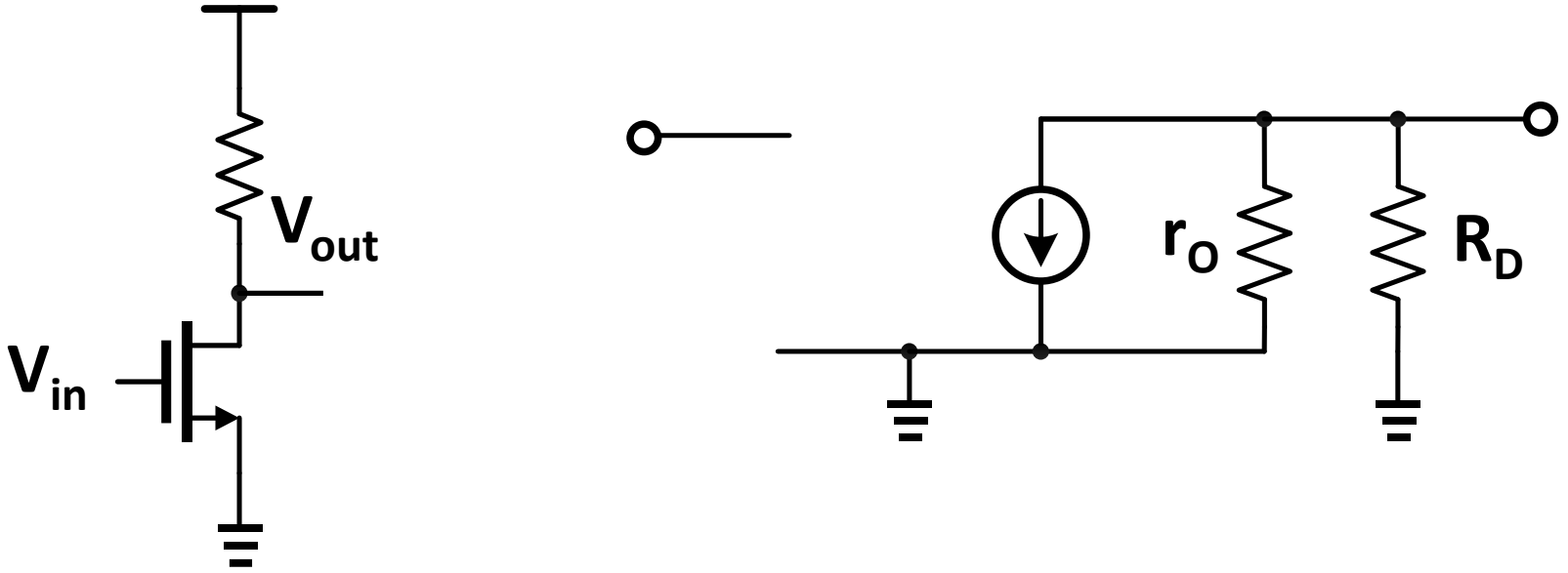
Multiple Stage Gain?

- How can you derive it? V_{out}/V_{in}.
- Gain is not everything. R_{in} and R_{out} matter significantly.



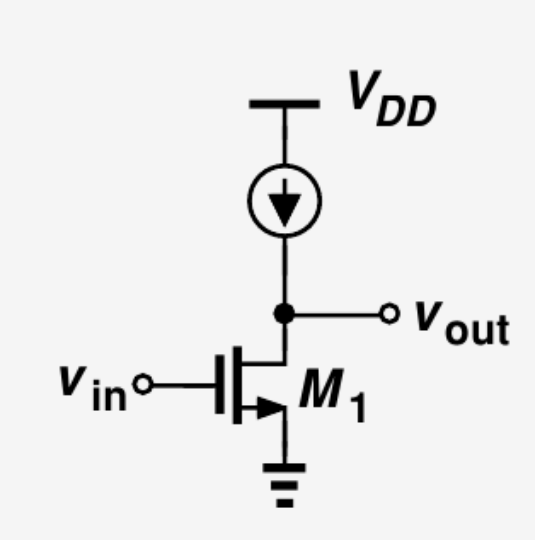
CS Amplifier

- Can you derive A_v, R_{in} and R_{out} in CS Amplifier?
- From now on, please see the three features at the same time.



Gain of CS Amp w/ Ideal Current Source

- Role of the current source is bias. What would be in the small signal world?
- What is Gain?

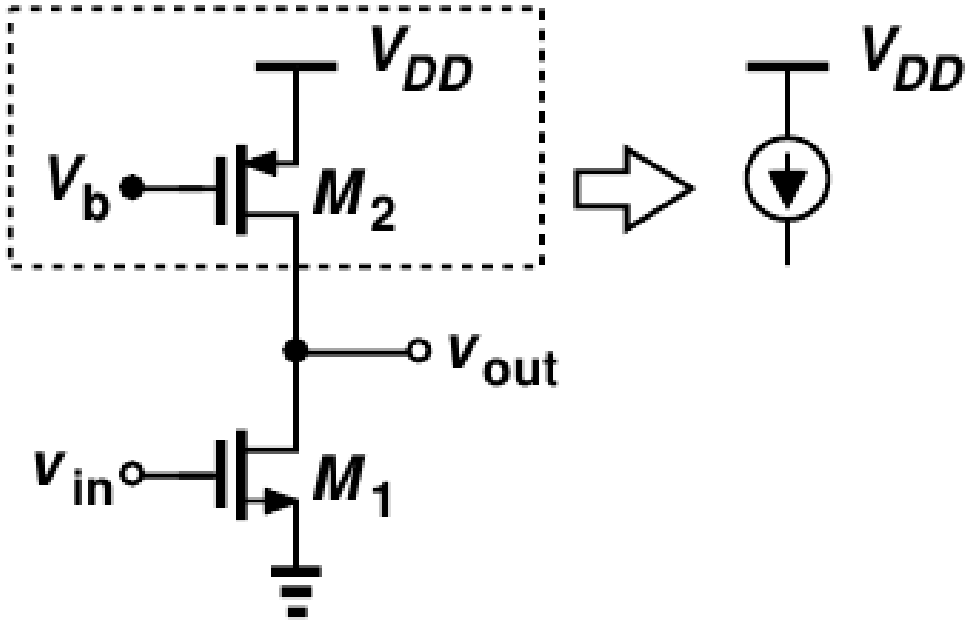


- How can you implement current source?

➔ We should define a current source specifically.

CS Amp w/ PMOS Current Source

- Gain? Rout?



Example 7.6

Figure 7.11 shows a PMOS CS stage using an NMOS current source load. Compute the voltage gain of the circuit.

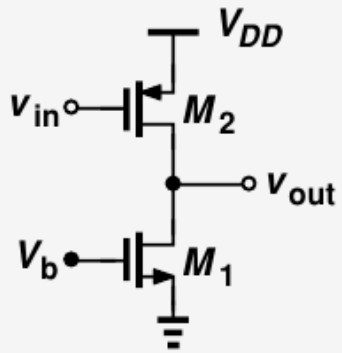
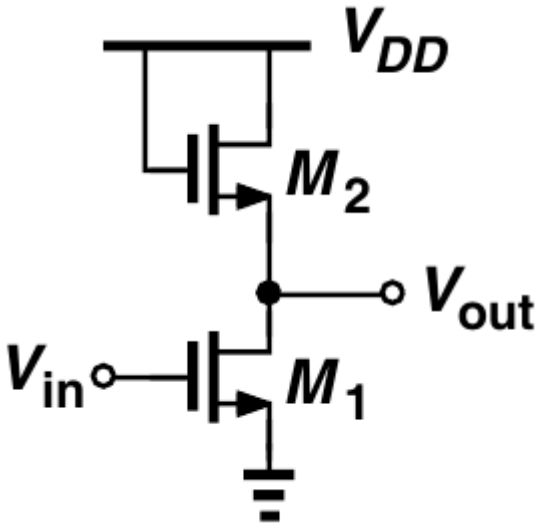


Figure 7.11 CS stage using an NMOS device as current source.

Dealing With PMOS

CS Stage w/ Diode-Connected Load

- Can you derive the resistance of M2 seen from source?



Example 7.7

Determine the voltage gain of the circuit shown in Fig. 7.13(a) if $\lambda \neq 0$.

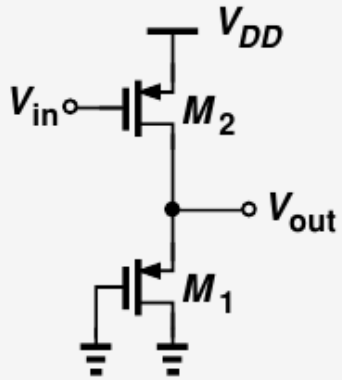
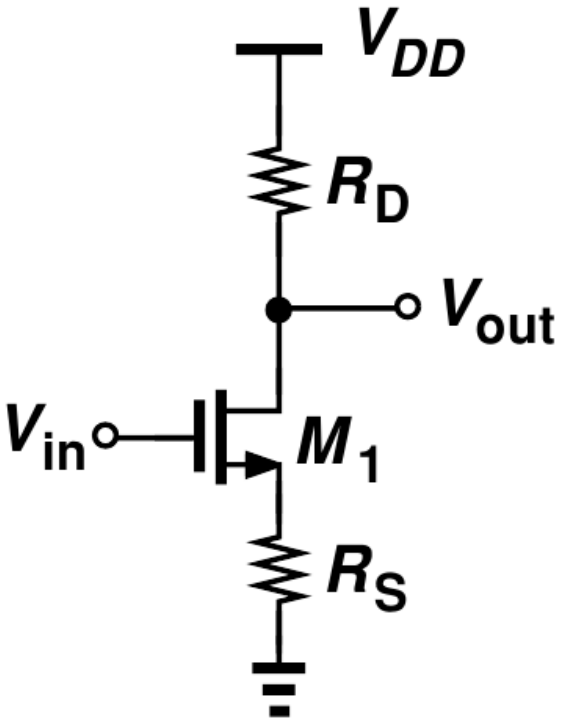
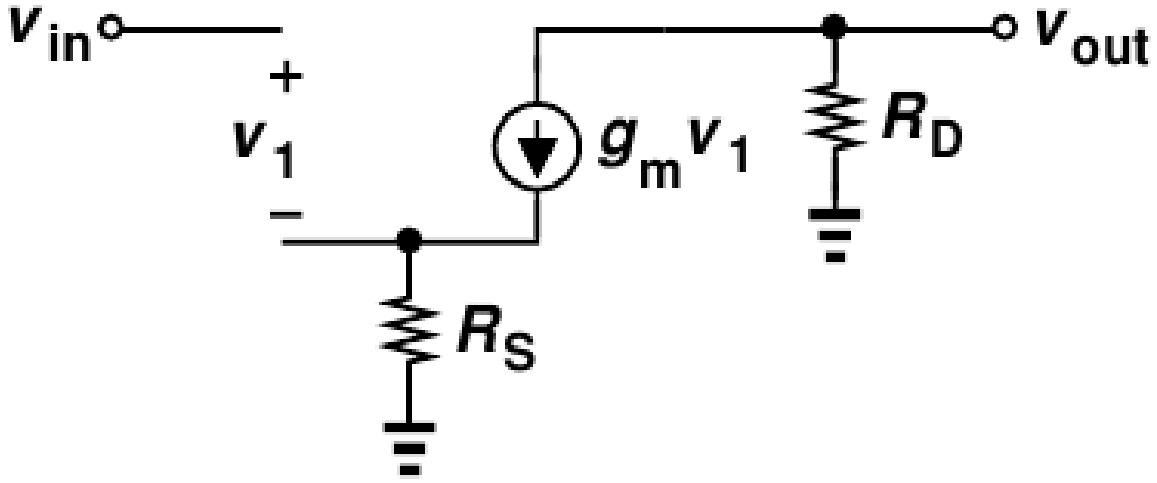


Figure 7.13 CS stage with diode-connected PMOS device.

CS Stage With Degeneration

- Gain?





Example 7.8

Compute the voltage gain of the circuit shown in Fig. 7.15(a) if $\lambda = 0$.

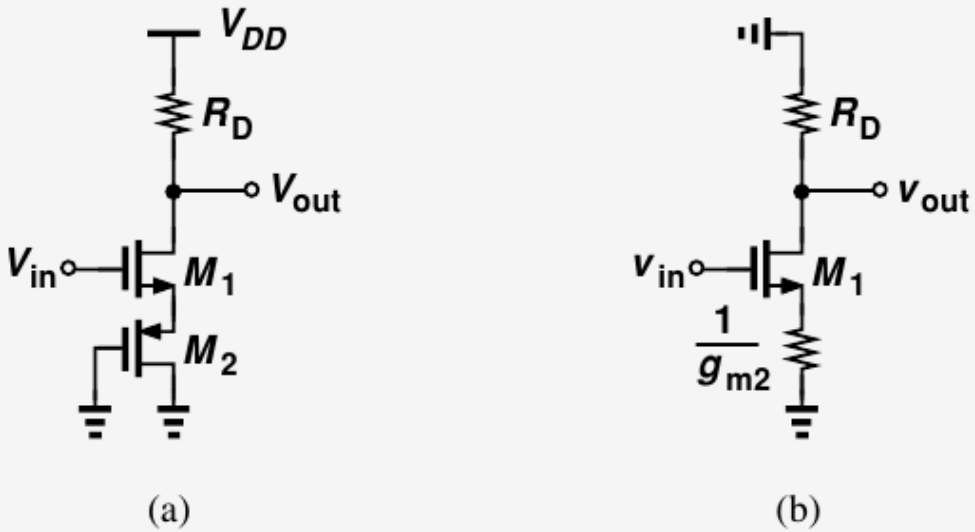
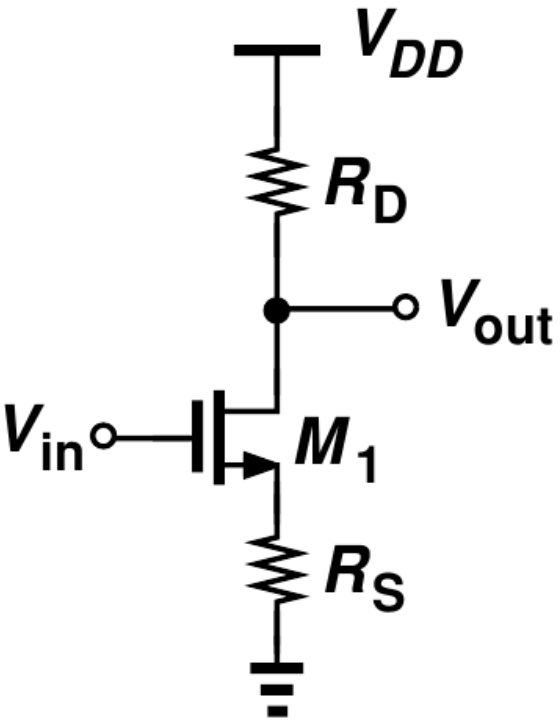
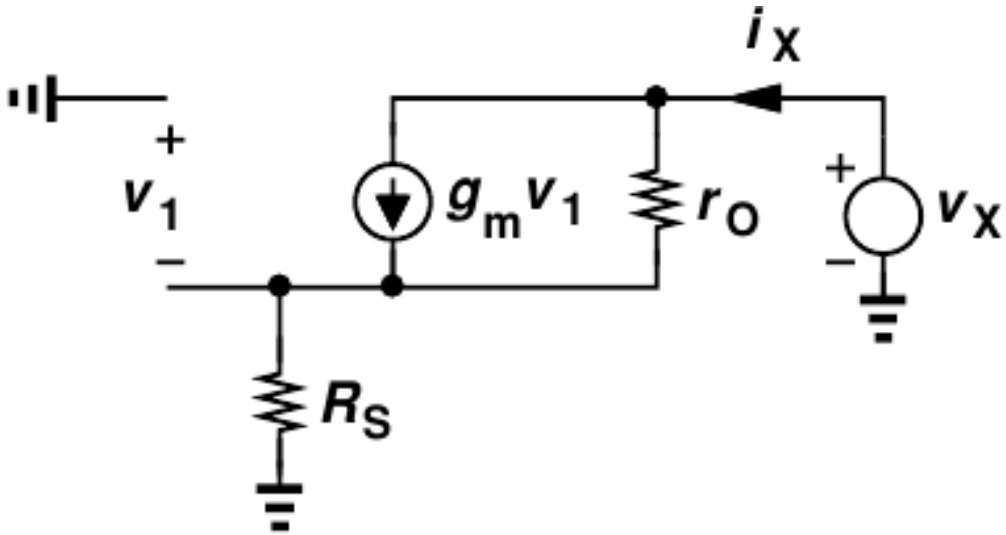


Figure 7.15 (a) Example of CS stage with degeneration, (b) simplified circuit.

Output Resistance?

- When λ = 0, it is simple. But what if λ ≠ 0?





Example 7.9

Compute the output resistance of the circuit in Fig. 7.18(a) if M_1 and M_2 are identical.

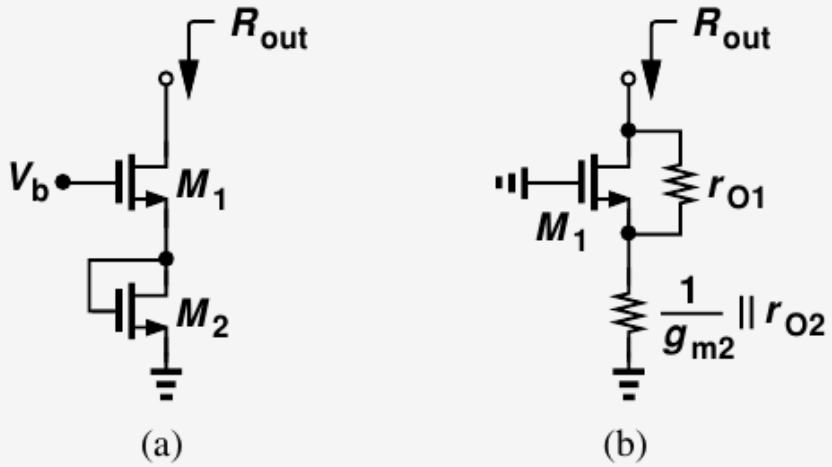


Figure 7.18 (a) Example of CS stage with degeneration, (b) simplified circuit.

Example 7.10

Determine the output resistance of the circuit in Fig. 7.19(a) and compare the result with that in the above example. Assume M_1 and M_2 are in saturation.

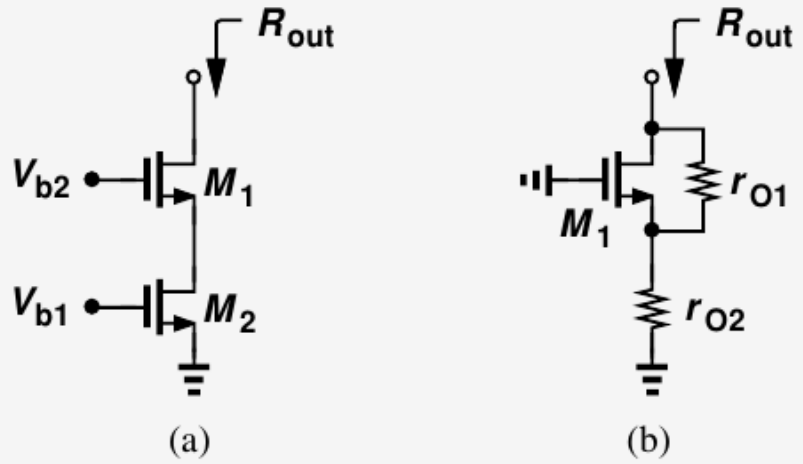


Figure 7.19 (a) Example of CS stage with degeneration, (b) simplified circuit.