Common Source Amplifier (3)

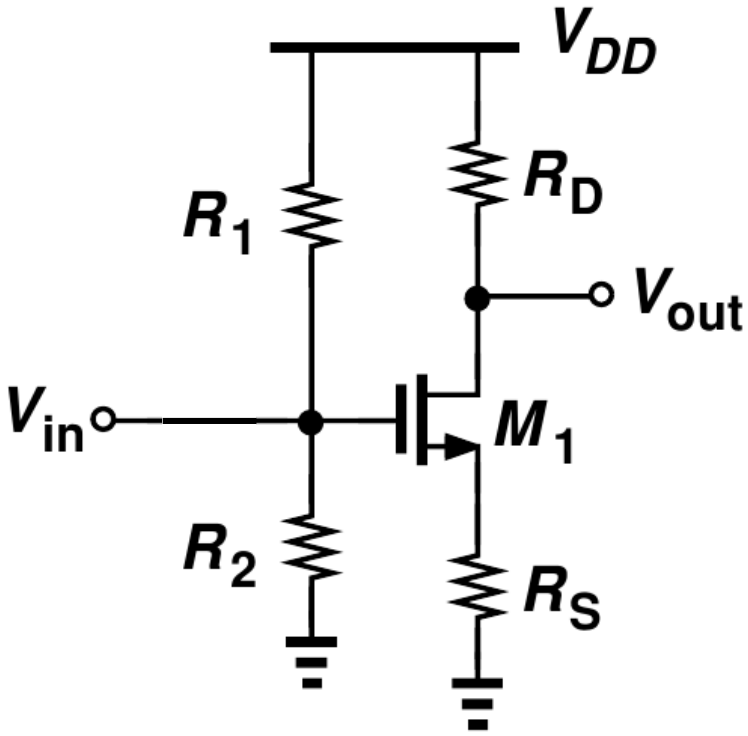
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Bias Circuit

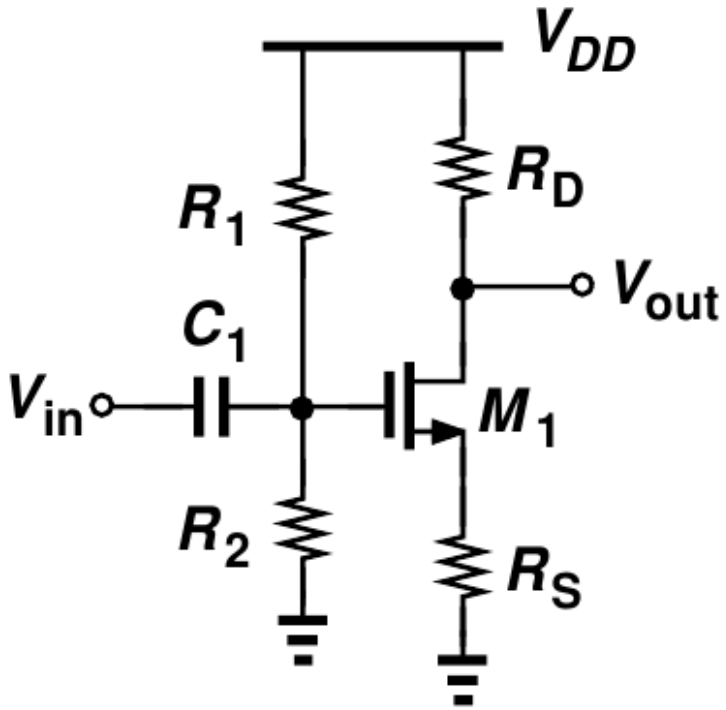
- How to achieve central input voltage condition? Like V_{IN} = 1V.
- We can use a voltage divider R_1 and R_2 as shown below.

➔ Then how can we apply v_{in}? You remember?



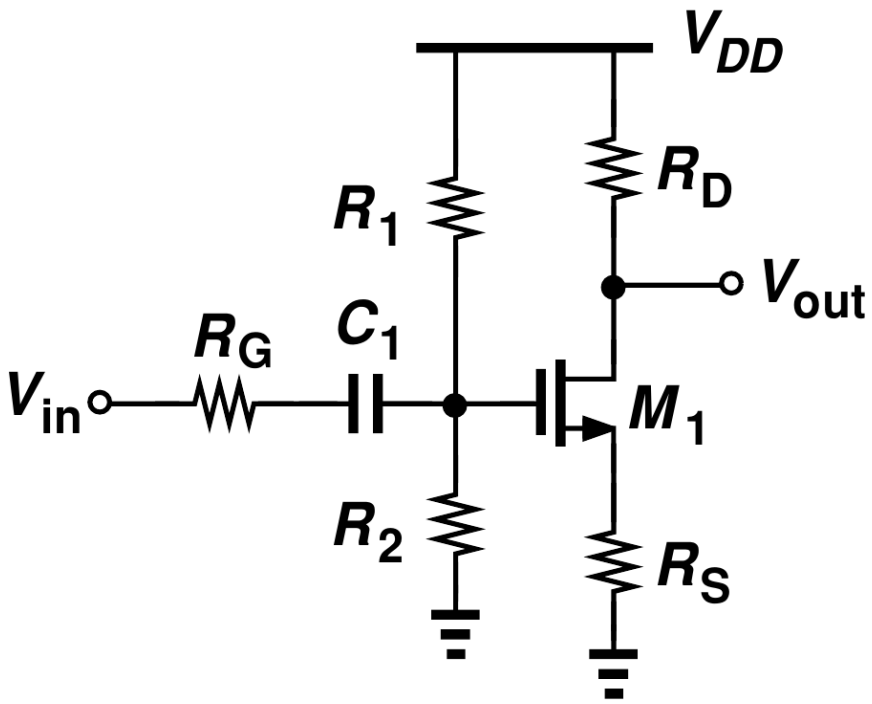
Bias Circuit w/ Coupling Capacitor

- Capacitor can be considered as a short-circuit for small signal while open circuit for DC bias signal (Why?)



Inclusion of Finite Source Impedance

- R_G and R_S degrade the gain



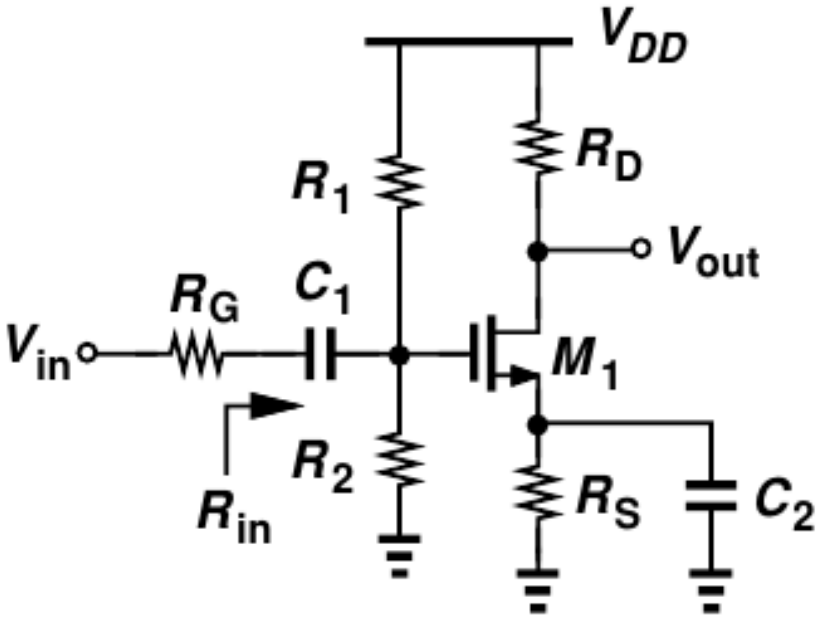
$$A_v = \frac{R_1||R_2}{R_G + R_1||R_2} \cdot \frac{-R_D}{\frac{1}{g_m} + R_S}$$

Why Do We Use R_S? Source Degeneration

- We use it for bias point stability.
- But, as you see, it degrades the gain.
- Is there any way for
  1) Removing the effect of R_S for small signal to obtain improved gain
  2) while keeping the effect of R_S for large signal bias

➔We have a useful element that reacts differently

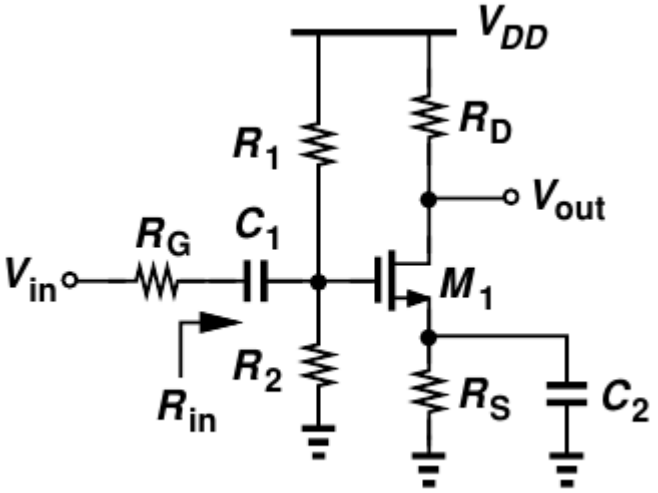
Use of a Bypass Capacitor

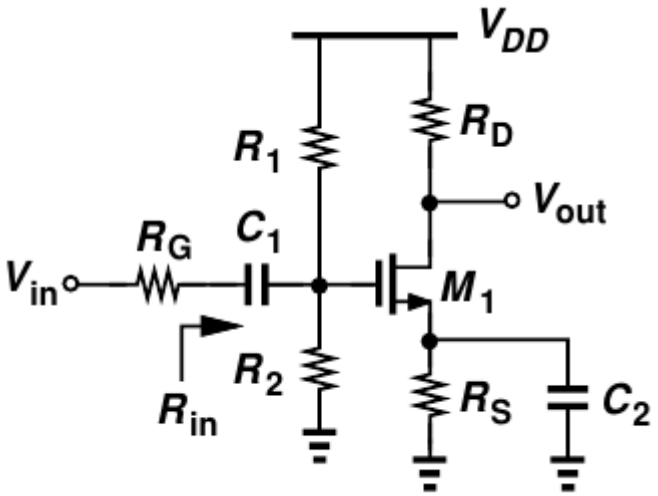


$$A_v = -\frac{R_1||R_2}{R_G + R_1||R_2} g_m R_D.$$

Example 7.11

Design the CS stage of Fig. 7.20(c) for a voltage gain of 5, an input impedance of 50 kΩ, and a power budget of 5 mW. Assume $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, $V_{TH} = 0.5\,\text{V}$, $\lambda = 0$, and $V_{DD} = 1.8\,\text{V}$. Also, assume a voltage drop of 400 mV across R_S.




V_{DD}
R_D
R_1
V_{out}
R_G
C_1
V_{in}
M_1
R_2
R_S
C_2
R_{in}