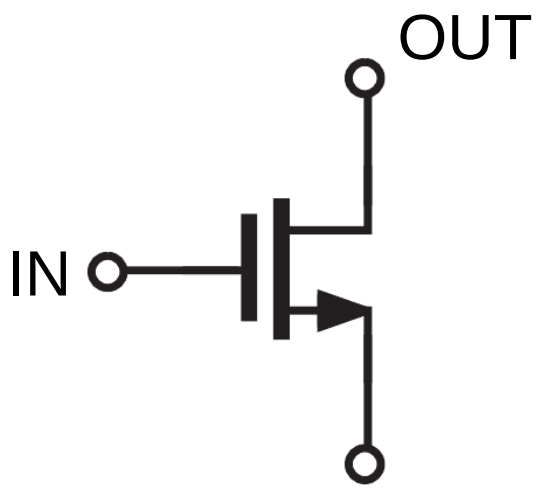
Common Gate Amplifier

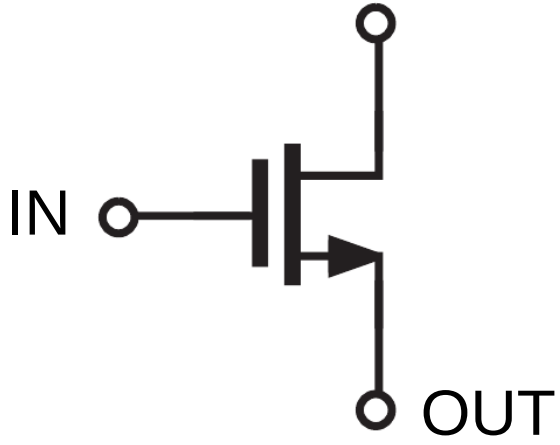
Hanwool Jeong

hwjeong@kw.ac.kr

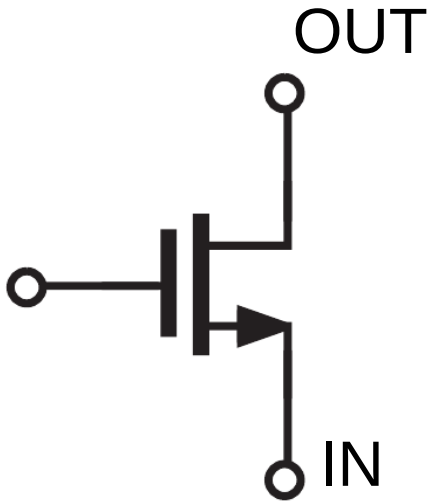
Possible Amplifier Configuration Using MOSFET



Common Source



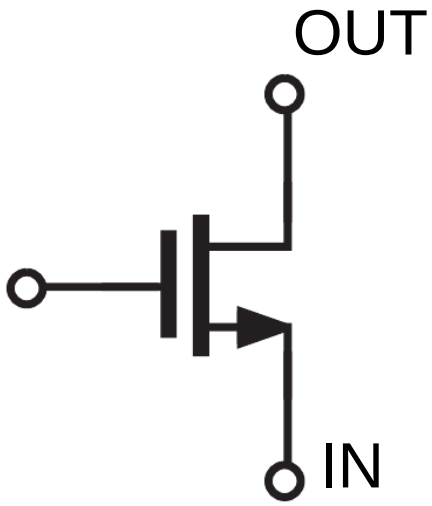
Common Drain
Source Follower



Common Gate

Common Gate Stage

- Why can we use it as an amplifier?
- How should the gate voltage be?
- Saturation or linear?
- How can OUT be captured as voltage?



Common Gate

Gain of CG Amplifier

- Considering $\Delta V_{in} = \Delta V_{GS}$ ➔ ΔI_{DS} ➔ Δv_{out} ,

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{\Delta I_{DS}}{-\Delta V_{GS}} \times \frac{\Delta V_{out}}{\Delta I_{DS}} = g_m \times R_D$$

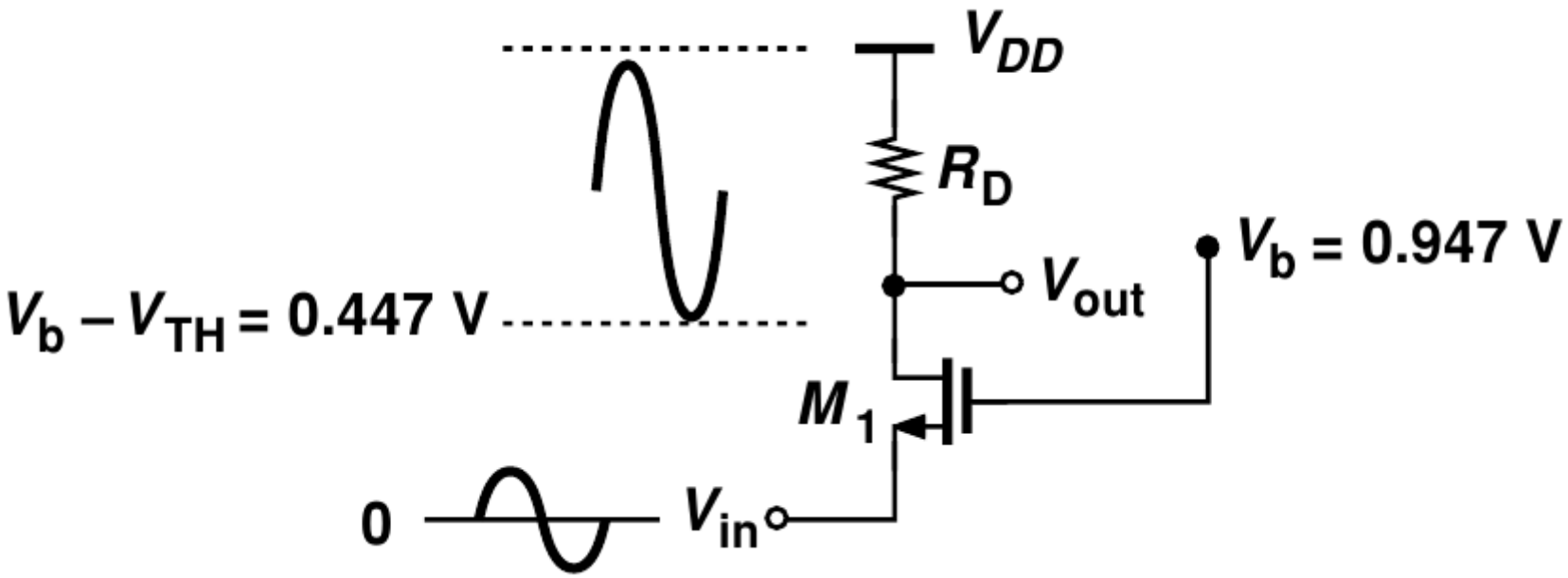
- Can you see the difference from CS amplifier?
- How can you achieve a large gain?
- Simply thinking, it is no surprise. But gain is everything? You should think of something else.

Example 7.12

A microphone having a dc level of zero drives a CG stage biased at $I_D = 0.5\,\text{mA}$. If $W/L = 50$, $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, $V_{TH} = 0.5\,\text{V}$, and $V_{DD} = 1.8\,\text{V}$, determine the maximum allowable value of R_D and hence the maximum voltage gain. Neglect channel-length modulation.

Example 7.12

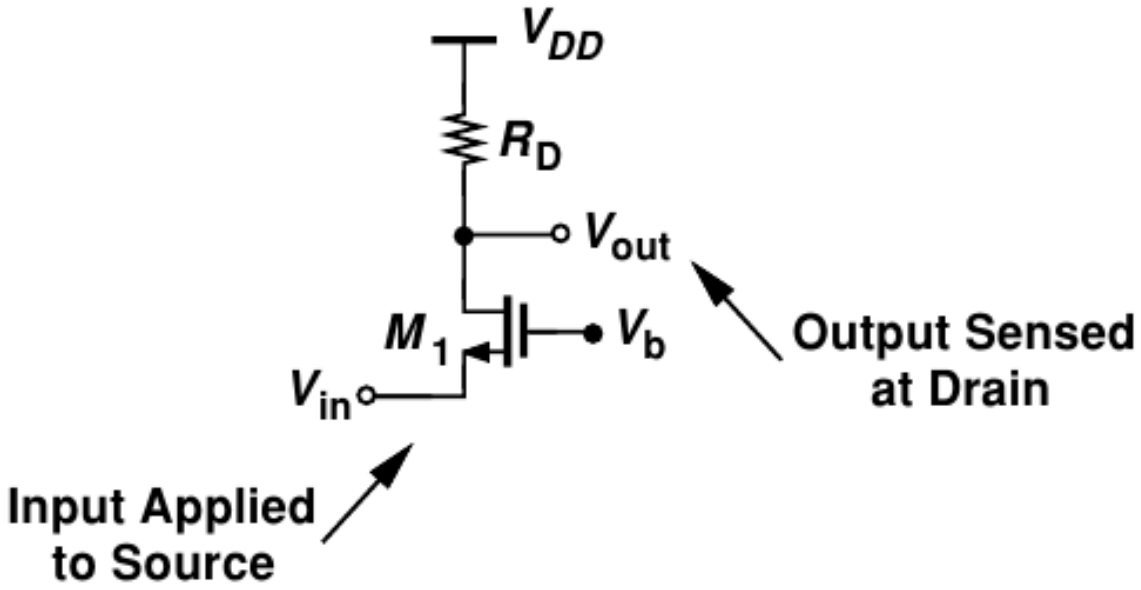
A microphone having a dc level of zero drives a CG stage biased at $I_D = 0.5\,\text{mA}$. If $W/L = 50$, $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, $V_{TH} = 0.5\,\text{V}$, and $V_{DD} = 1.8\,\text{V}$, determine the maximum allowable value of R_D and hence the maximum voltage gain. Neglect channel-length modulation.



Most Noticeable Difference from CS Amplifier is

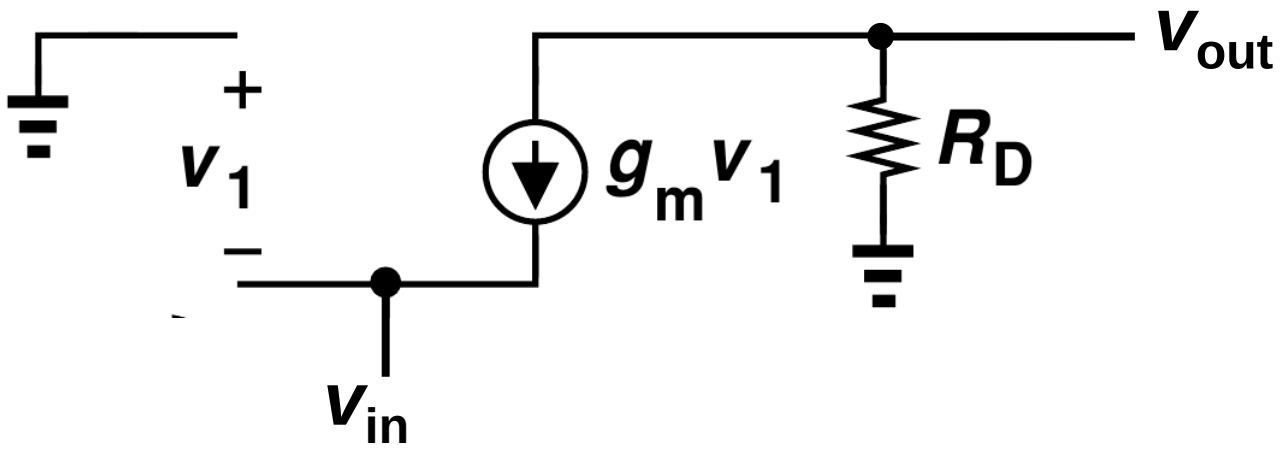
- Output current flows through input node

➔ How does it affect to amplifier performance?

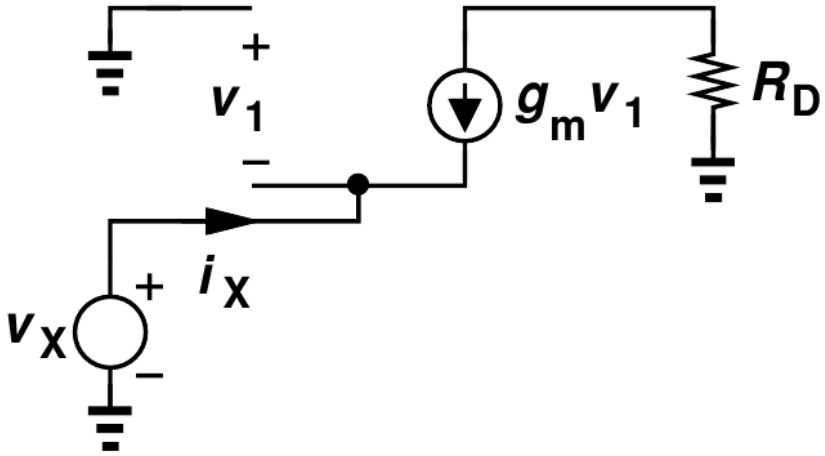


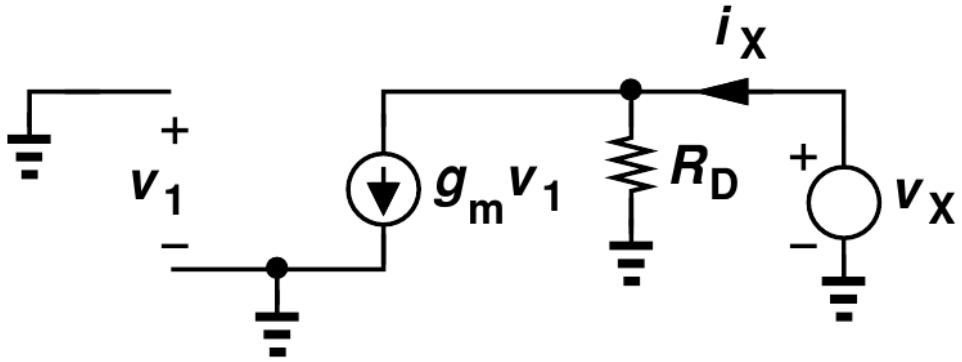
Small Signal Model of CG Amplifier

- Can you find gain from small signal model?

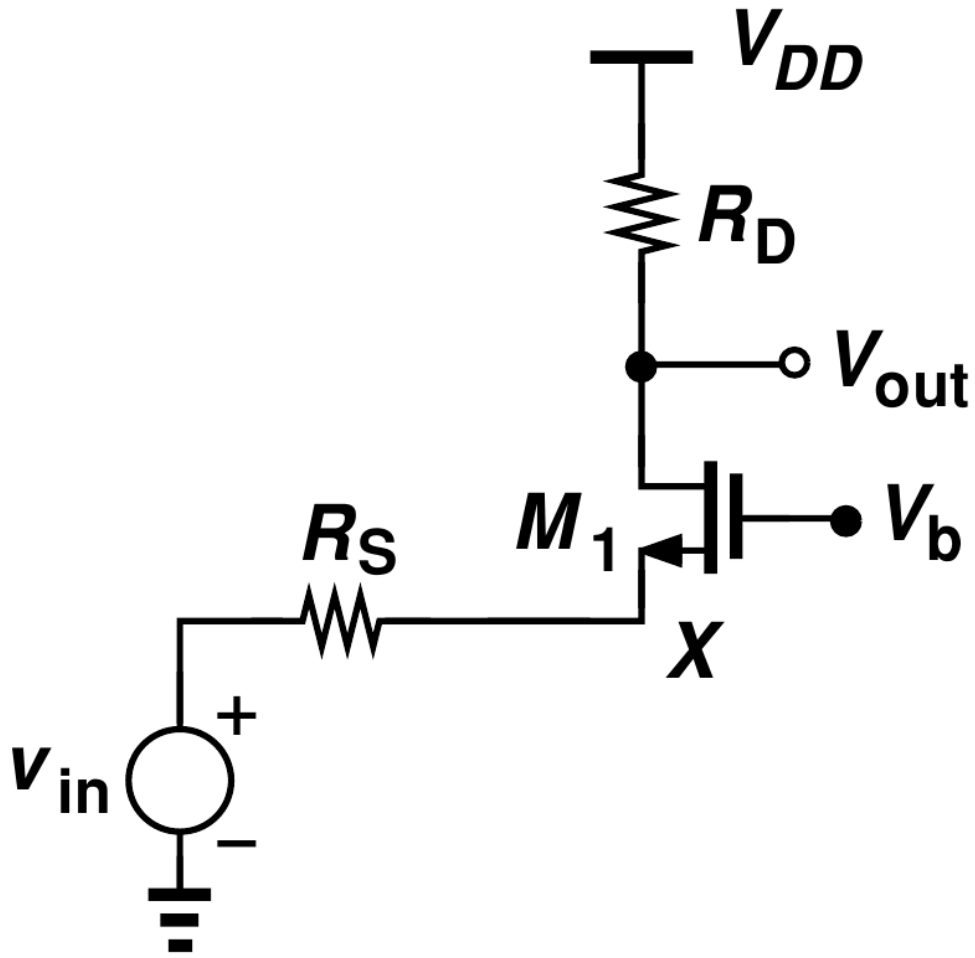


R_{in} & R_{out}

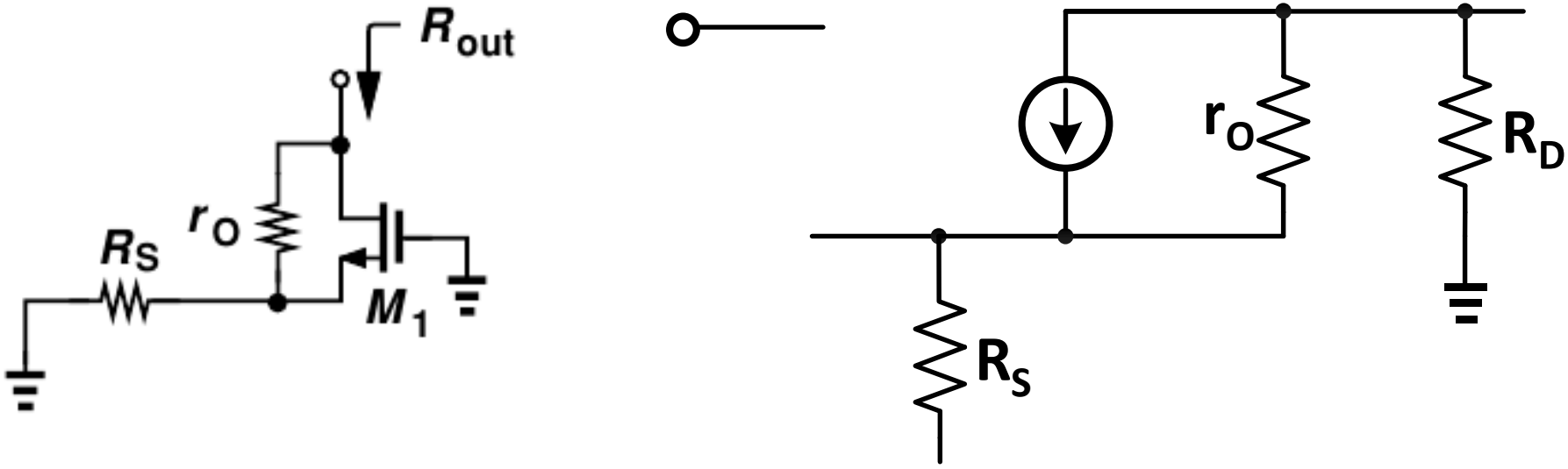




Considering Finite Source Resistance



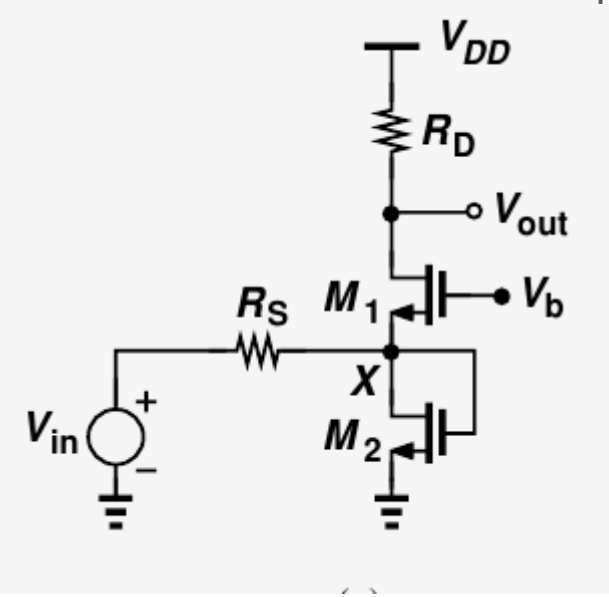
R_{out} when $\lambda \neq 0$



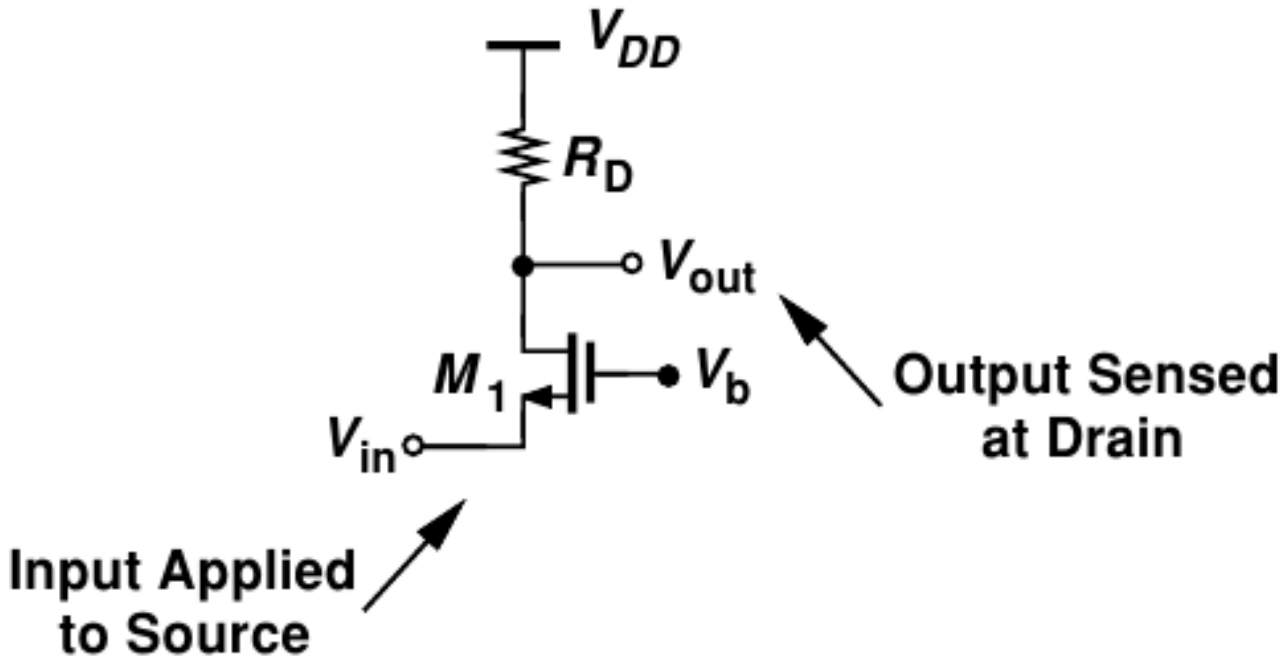
$$R_{out} = (1 + g_m r_O) R_S + r_O$$

Example 7.13

For the circuit shown in Fig. 7.26(a), calculate the voltage gain if $\lambda = 0$ and the output impedance if $\lambda > 0$.

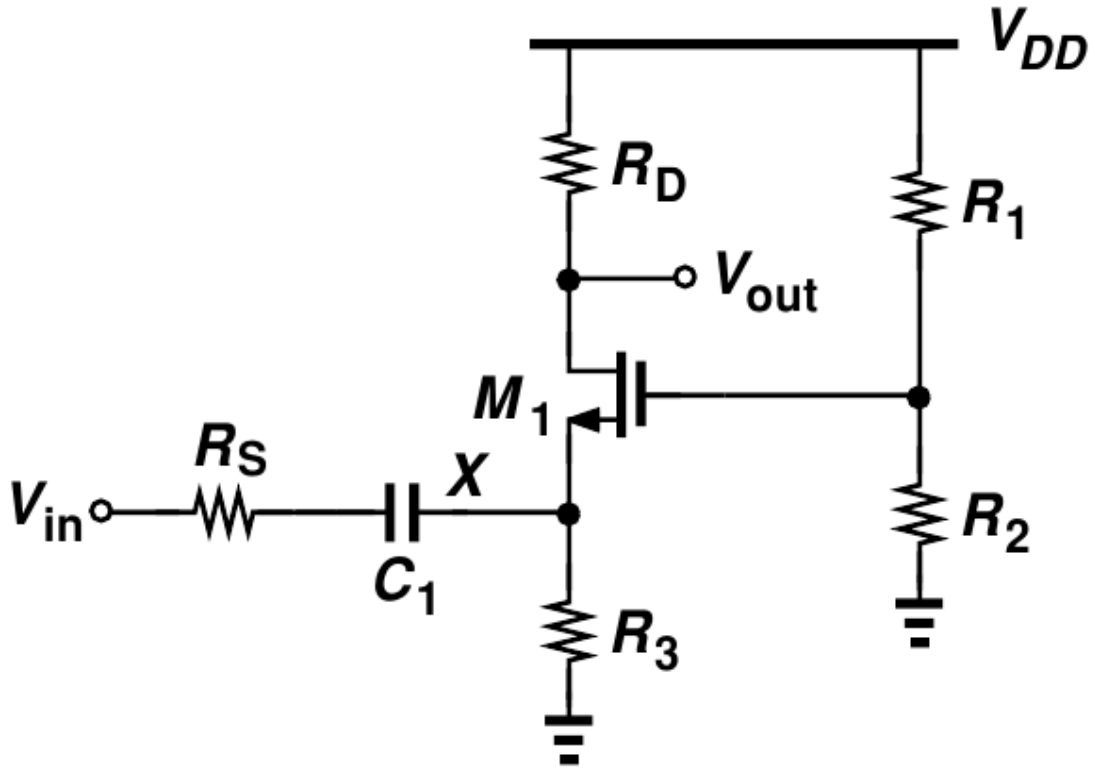


How Can You Bias CG Stage?



CG Stage w/ Biasing

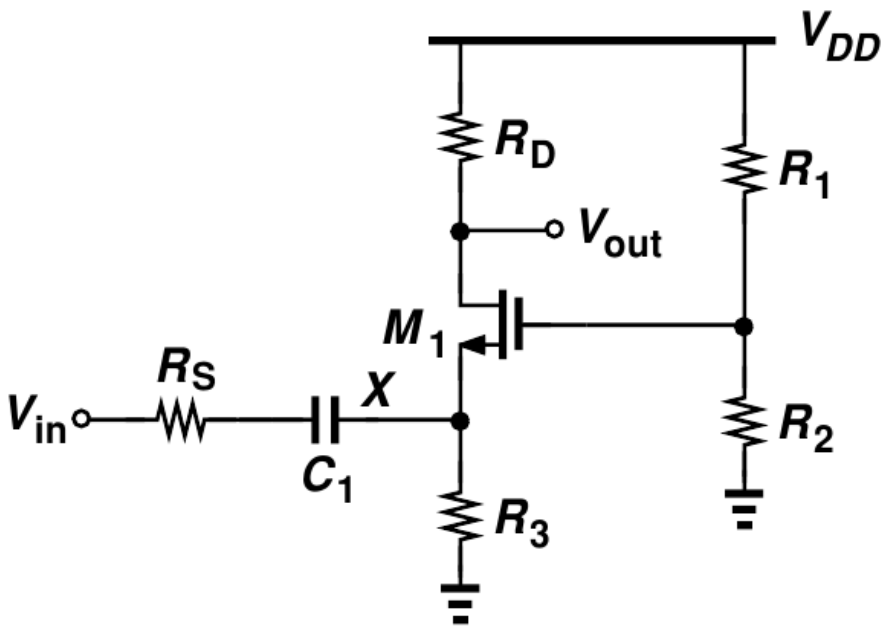
- Gain?



Example 7.14

Design the common-gate stage of Fig. 7.27 for the following parameters: $v_{out}/v_{in} = 5, R_S = 0, R_3 = 500\,\Omega, 1/g_m = 50\,\Omega$, power budget $= 2\,\text{mW}, V_{DD} = 1.8\,\text{V}$. Assume $\mu_n C_{ox} = 100\,\mu\text{A/V}^2, V_{TH} = 0.5\,\text{V}$, and $\lambda = 0$.

- Allocate ~10μA to R_1-R_2 divider



Example 7.15

Suppose in Example 7.14, we wish to minimize W/L (and hence transistor capacitances). What is the minimum acceptable value of W/L?