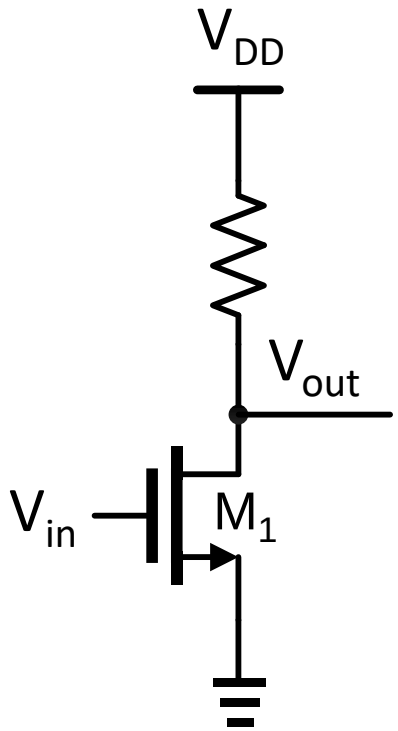
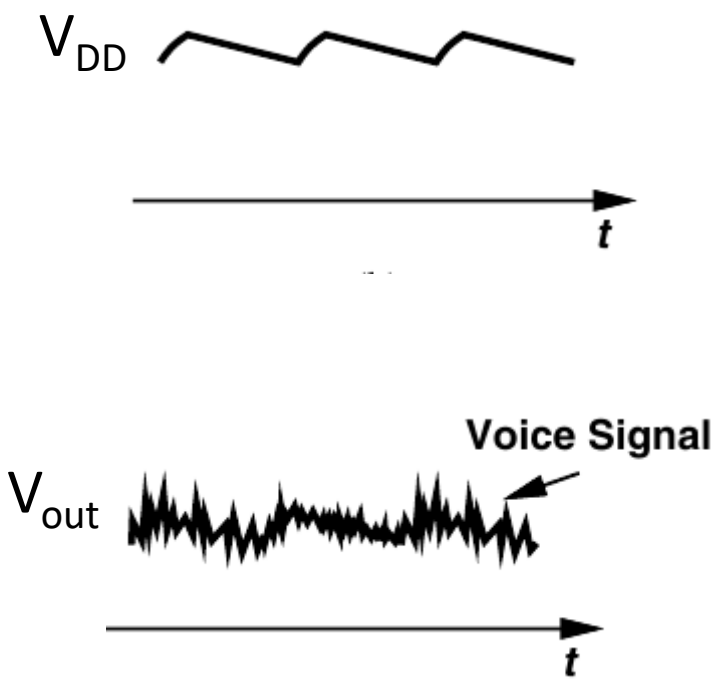
Effect of Supply Noise

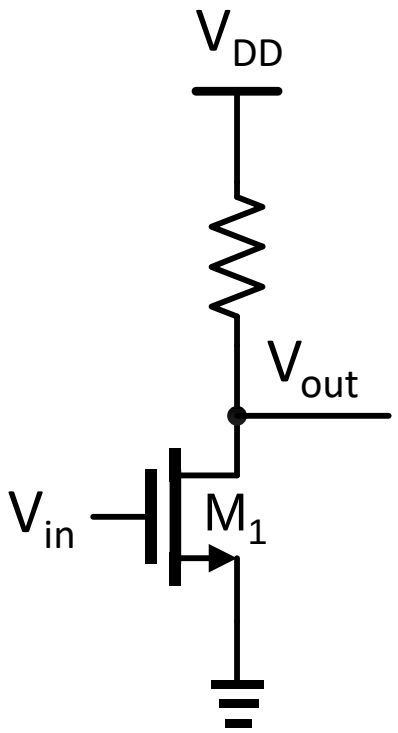
- What if there is a ripple on V_{DD}?

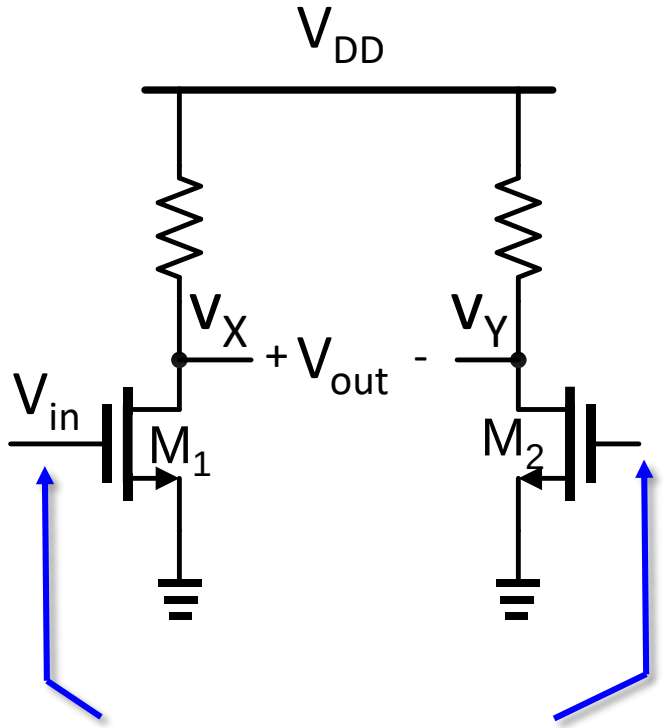




Making Reference Node Have the Same Ripple

- Can be free from the supply ripple (Can you derive v_X & v_Y?)



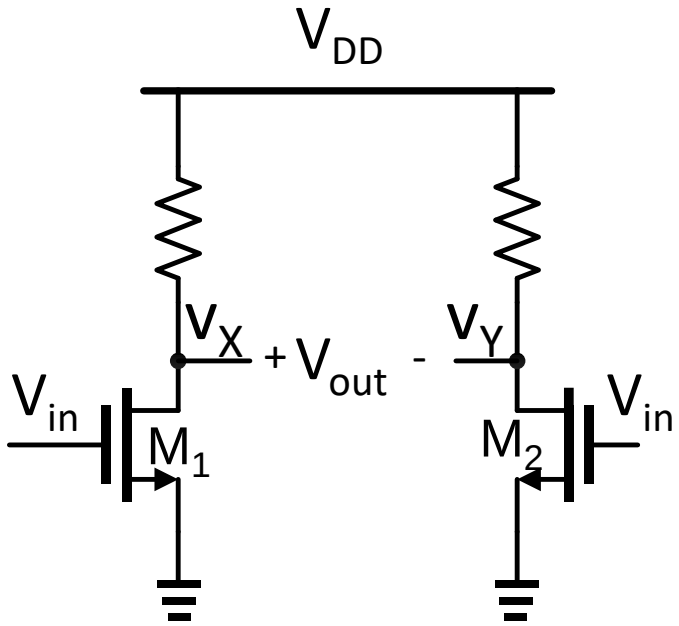


Bias to the same voltage

➔ Yet, M2 wastes the current. Can't we use it for amplifying?

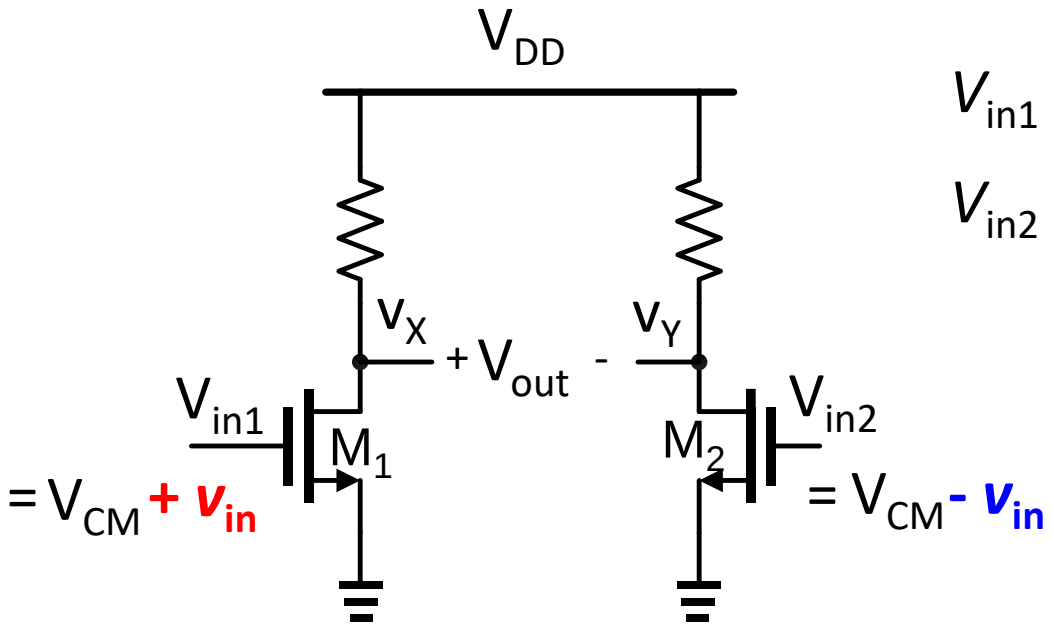
Applying Signals to Two MOSFETs

- $v_X = v_Y$ ➔ V_{out} is kept zero ➔ No use.



Differential Signals

- Can you derive Vout?



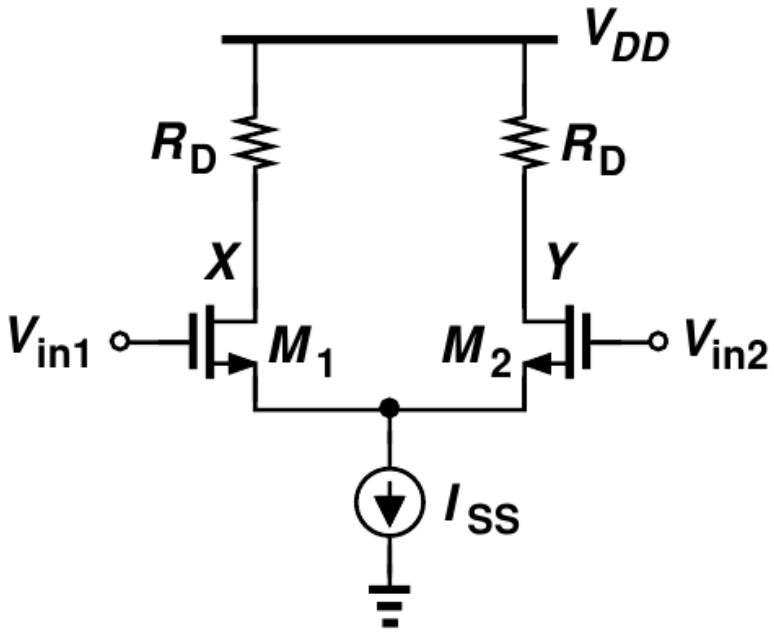
$$V_{in1} = V_0 \sin \omega t + V_{CM}$$

$$V_{in2} = -V_0 \sin \omega t + V_{CM}$$

- V_{in1} and V_{in2} has the common value of DC voltage, so we call it as “common-mode (CM)” level, V_{CM}

Resultant Structure

- Symmetric in R and MOSFET. Input ac signal only differs.
- Tail current source? ➔ For biasing effectively.



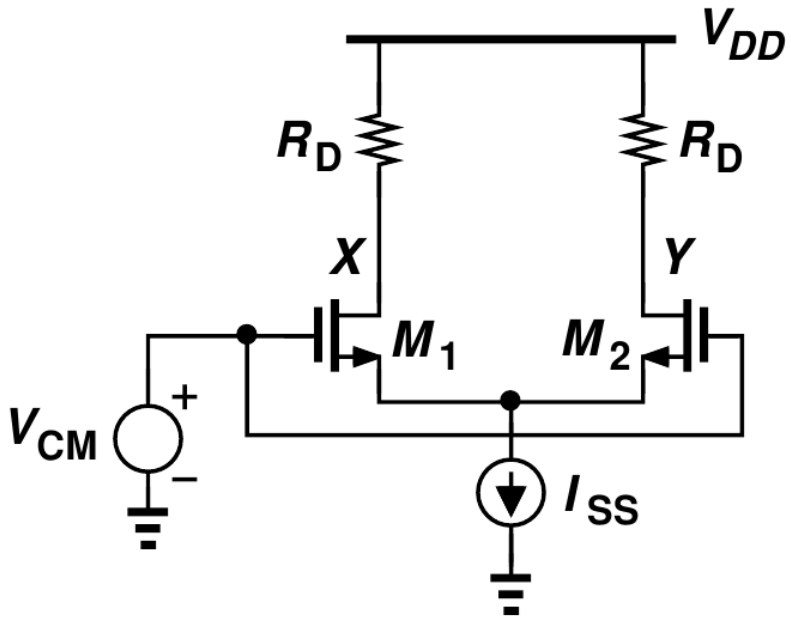
MOSFET Differential Pair

Hanwool Jeong

hwjeong@kw.ac.kr

Biasing with Current Source

- We can start from assuming current source is ideal.



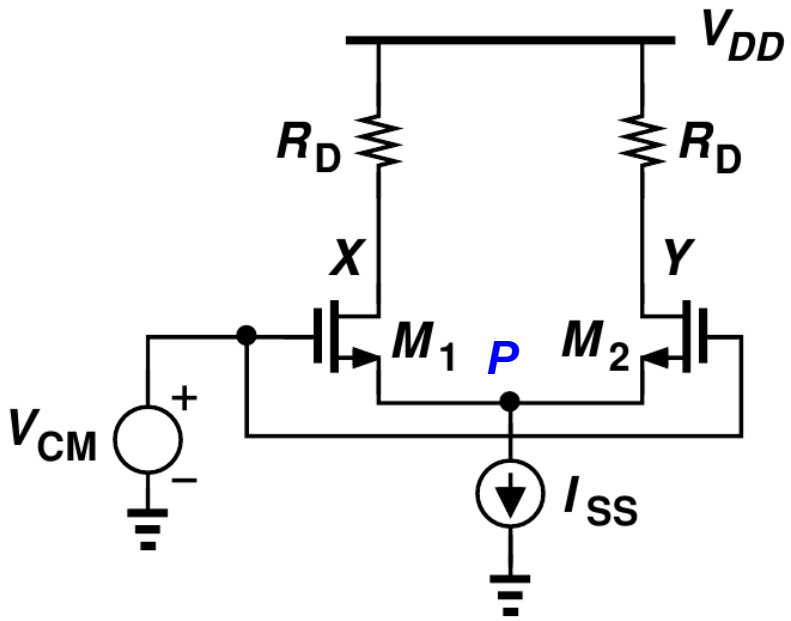
$$V_X = V_Y = V_{DD} - R_D \frac{I_{SS}}{2}$$

= Output CM level

$$I_{D1} = I_{D2} = \frac{I_{SS}}{2}$$

How About Effect of VCM on Bias Current?

- Can we say it is $I_{SS}/2$ without considering the effect of V_{CM}?



Equilibrium over-drive voltage

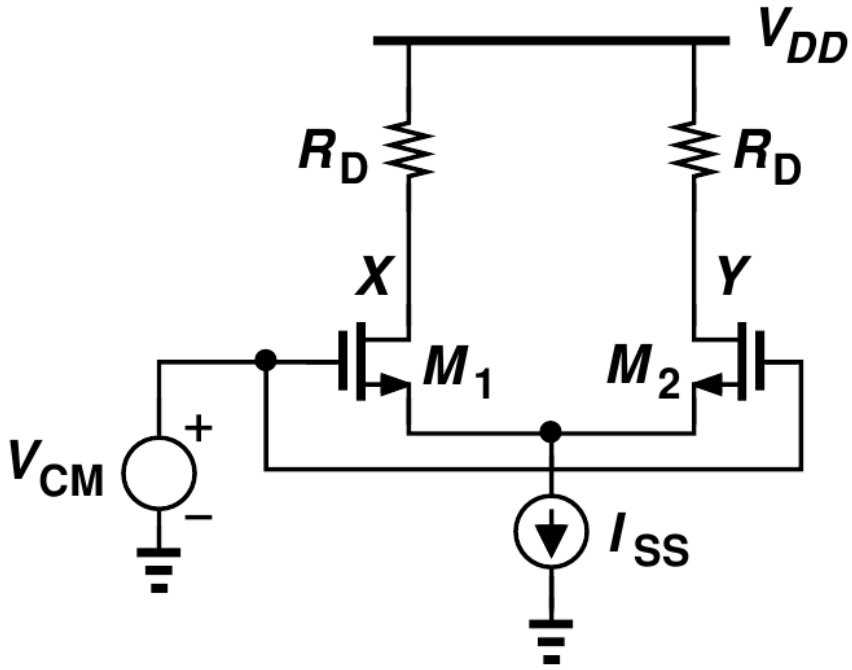
$$(V_{GS} - V_{TH})_{equil.} = \sqrt{\frac{I_{SS}}{\mu_n C_{ox} \frac{W}{L}}}$$

- P node is adjusted to hold

$$\frac{I_{SS}}{2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{th})$$

CM Variation Rejection

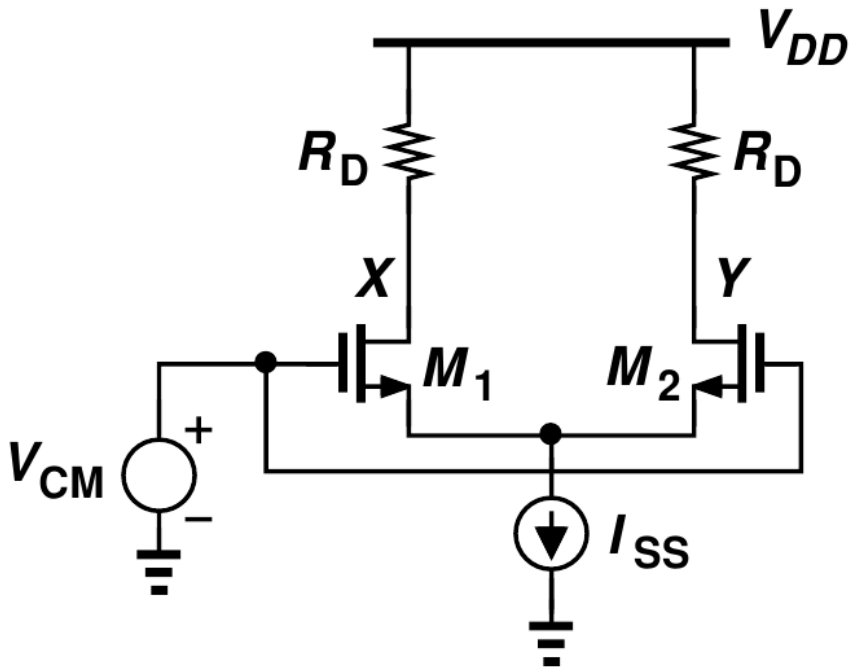
- A Change in V_{CM} cannot alter $I_{D1} = I_{D2} = I_{SS/2}$, leaving V_X and V_Y undisturbed.
- We say the circuit thus rejects input CM variation.



Saturation Region Constraint

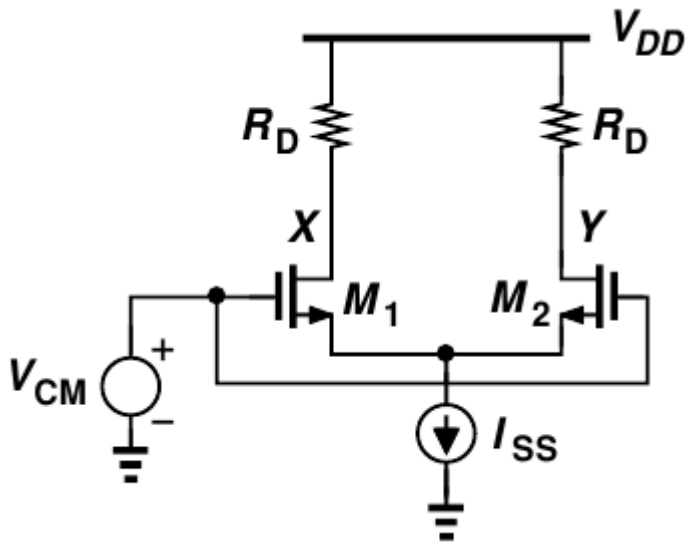
- What is the condition to make MOSFET keep in the saturation region?

$$V_{DD} - R_D \frac{I_{SS}}{2} > V_{CM} - V_{TH}$$



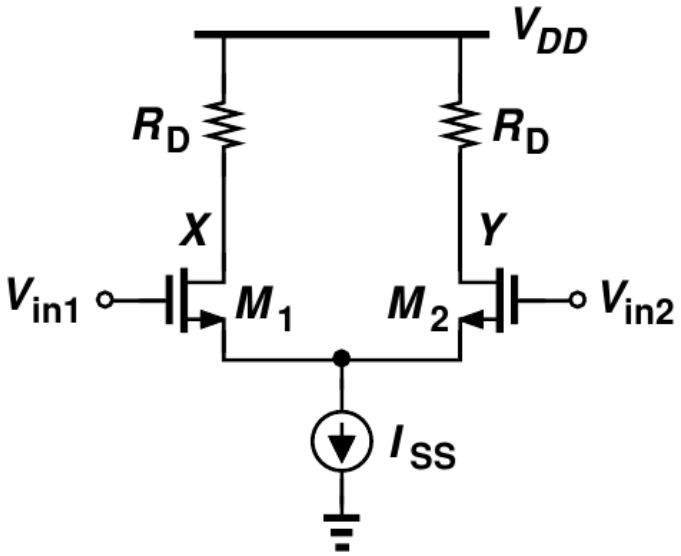
Example 10.15

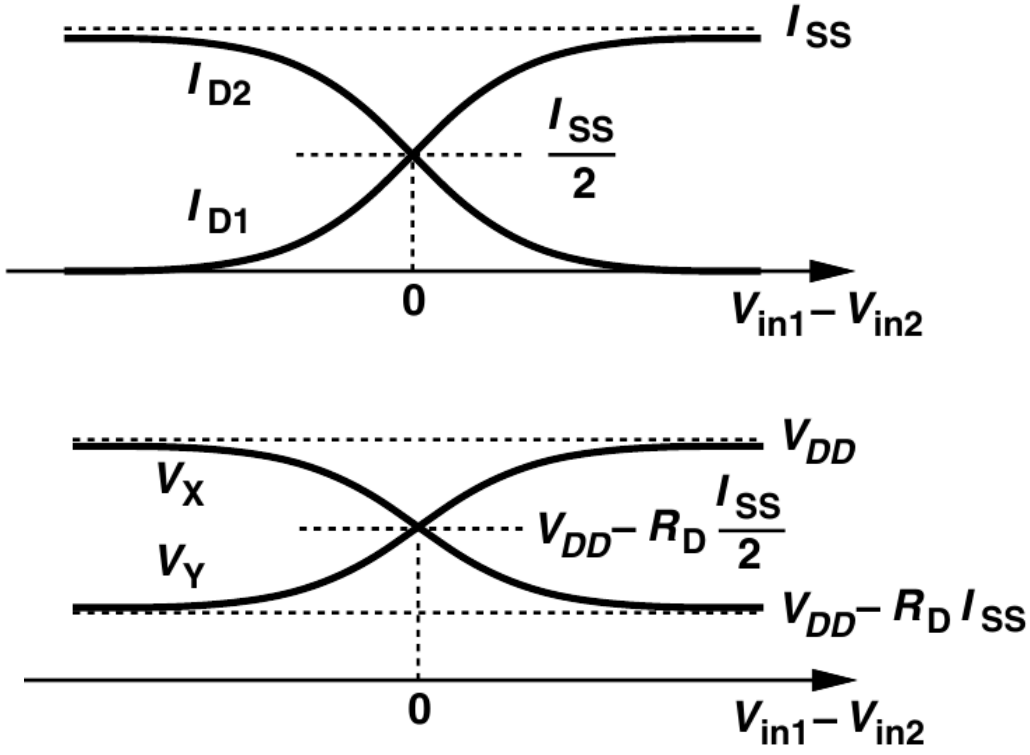
A MOS differential pair is driven with an input CM level of 1.6 V. If $I_{SS} = 0.5\,\text{mA}$, $V_{TH} = 0.5\,\text{V}$, and $V_{DD} = 1.8\,\text{V}$, what is the maximum allowable load resistance?



Response to Differential Voltage Input

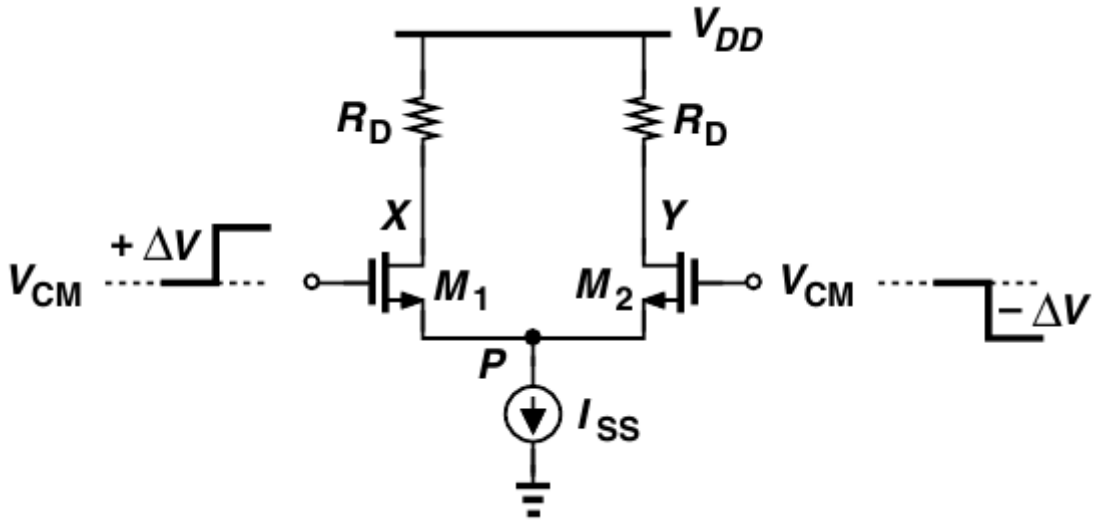
- Differential pair amplifies the voltage difference between V_{in1} and V_{in2}. It is convenient to define $v_{in} = V_{in1} - V_{in2}$
- How does the current and voltage response to v_{in} change?





Gain of Differential MOSFET Pair

- Now, small signal voltage ΔV is observed at V_{in1} and V_{in2} in the opposite phases.



$$\Delta I_{D1} = g_m \Delta V \qquad \Delta I_{D2} = -g_m \Delta V$$

$$\Delta V_X - \Delta V_Y = -2 g_m R_D \Delta V.$$

$$A_v = -g_m R_D.$$

Example 10.16

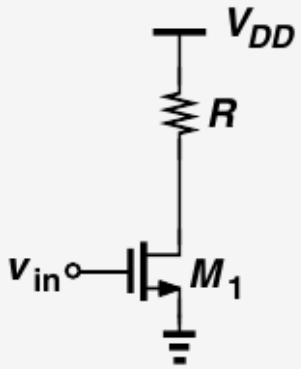
Design an NMOS differential pair for a voltage gain of 5 and a power budget of 2 mW subject to the condition that the stage following the differential pair requires an input CM level of at least 1.6 V. Assume $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, $\lambda = 0$, and $V_{DD} = 1.8\,\text{V}$.

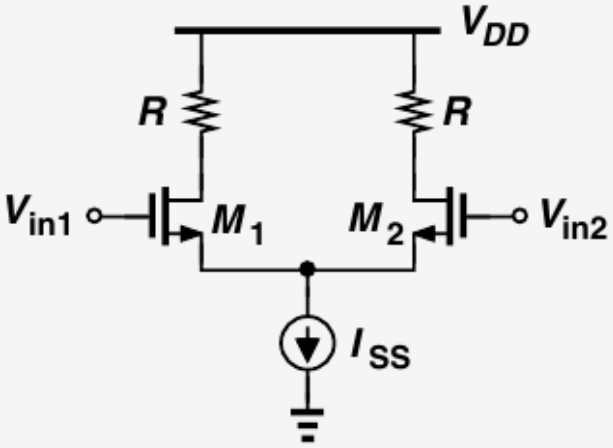
Example 10.17

What is the maximum allowable input CM level in the previous example if $V_{TH} = 0.4$ V?

Example 10.18

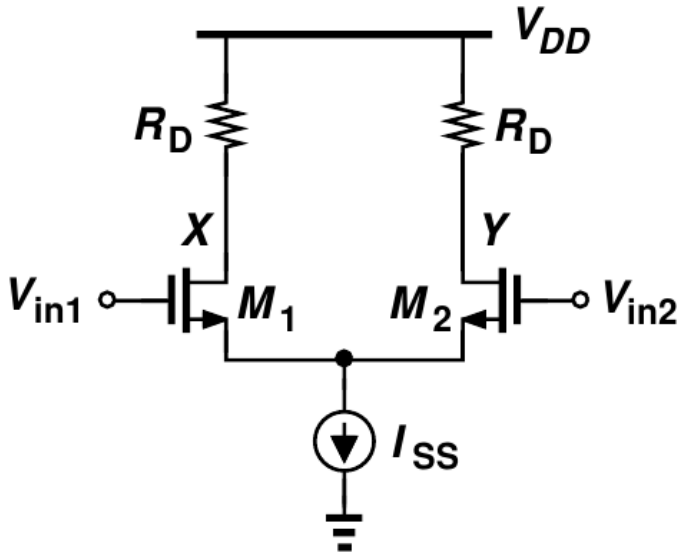
The common-source stage and the differential pair shown in Fig. 10.28 incorporate equal load resistors. If the two circuits are designed for the same voltage gain and the same supply voltage, discuss the choice of (a) transistor dimensions for a given power budget, (b) power dissipation for given transistor dimensions.

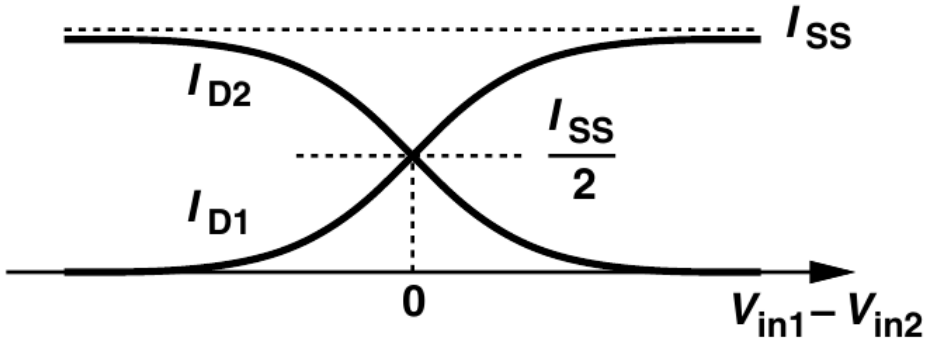




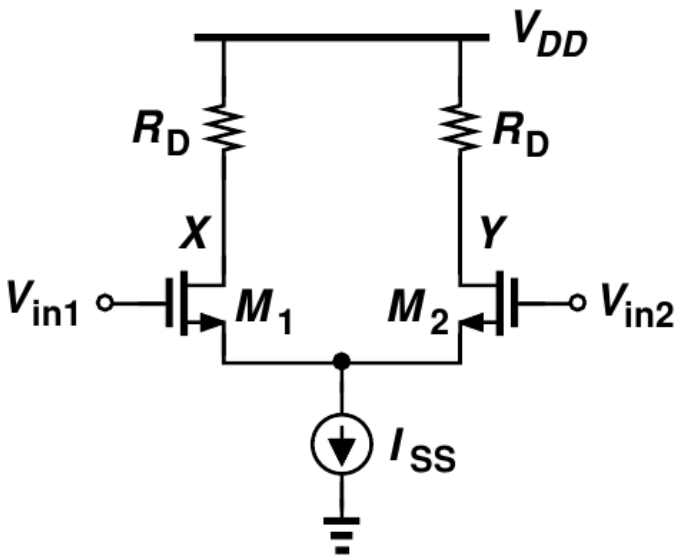
Range of $v_{in} = V_{in1} - V_{in2}$

- Revisit followings.





- It seems that there is a range constraint for v_{in} for linearity.
- We can find the mathematical term that relates I_D vs. v_{in}



$$V_{in1} - V_{in2} = V_{GS1} - V_{GS2}$$

$$= \sqrt{\frac{2}{\mu_n C_{ox} \frac{W}{L}}}(\sqrt{I_{D1}} - \sqrt{I_{D2}})$$

$$(V_{in1} - V_{in2})^2 = \frac{2}{\mu_n C_{ox} \frac{W}{L}}(I_{SS} - 2\sqrt{I_{D1} I_{D2}})$$

Utilizing $I_{D2} = I_{SS} - I_{D1}$,

$$I_{D1} = \frac{I_{SS}}{2} + \frac{V_{in1} - V_{in2}}{4}\sqrt{\mu_n C_{ox} \frac{W}{L}\left[4I_{SS} - \mu_n C_{ox} \frac{W}{L}(V_{in1} - V_{in2})^2\right]}$$

$$I_{D2} = \frac{I_{SS}}{2} + \frac{V_{in2} - V_{in1}}{4}\sqrt{\mu_n C_{ox} \frac{W}{L}\left[4I_{SS} - \mu_n C_{ox} \frac{W}{L}(V_{in2} - V_{in1})^2\right]}$$

$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox} \frac{W}{L}} - (V_{in1} - V_{in2})^2}.$$

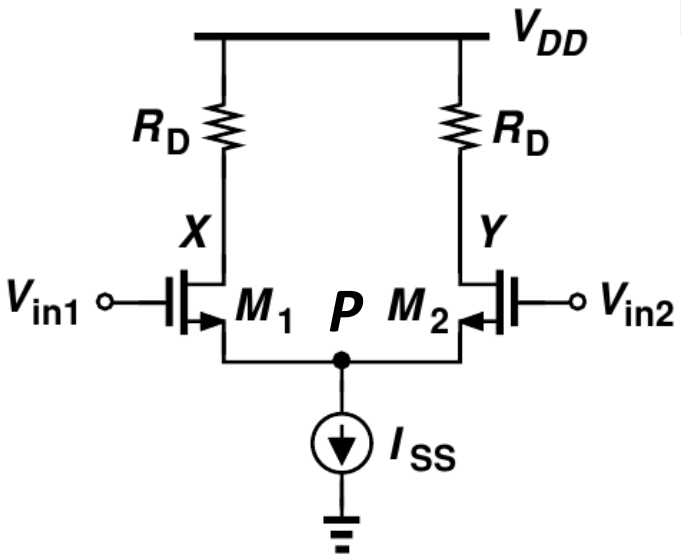
Small Signal Constraint

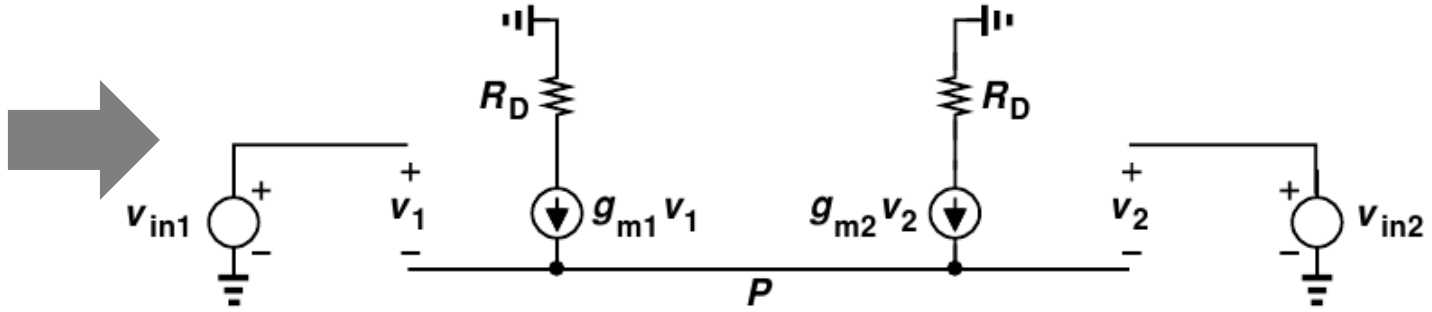
$$|V_{in1} - V_{in2}| \ll \frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}},$$

$$I_{D1} - I_{D2} \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}$$

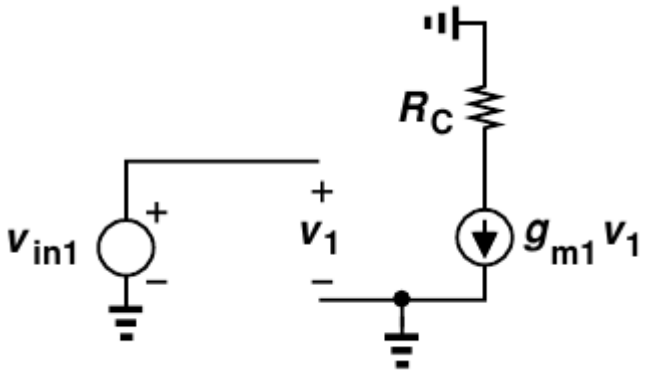
$$= \sqrt{\mu_n C_{ox}\frac{W}{L}I_{SS}}(V_{in1} - V_{in2}).$$

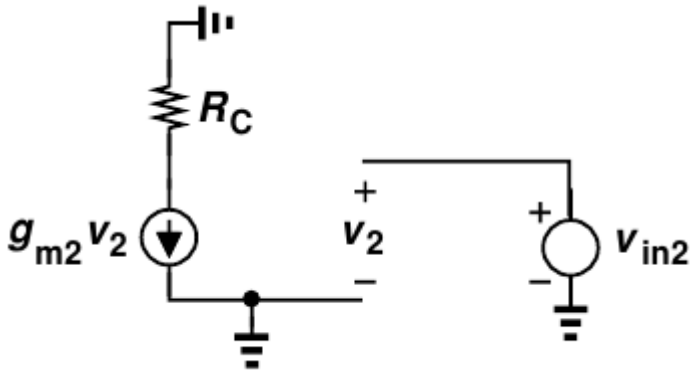
Small Signal Model



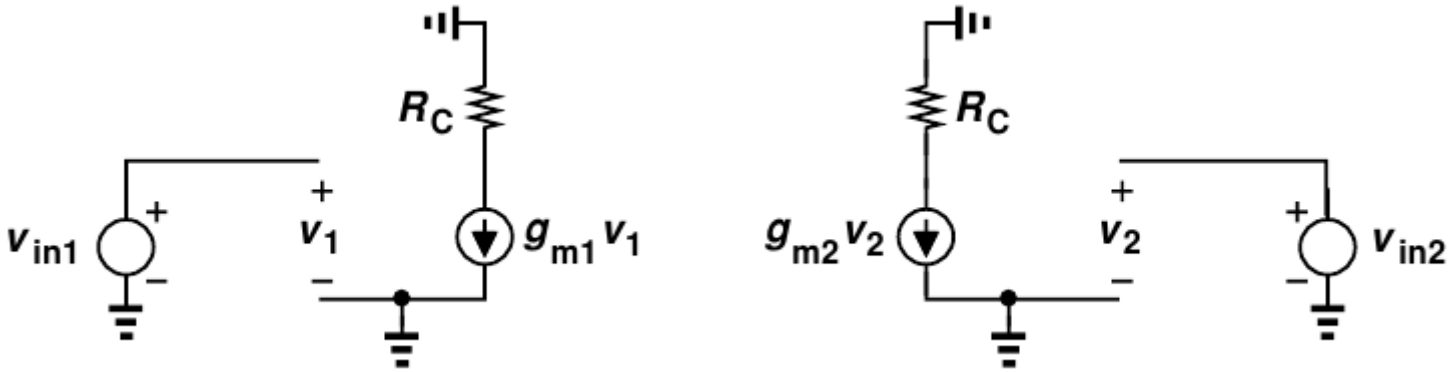


$v_1 = -v_2$





You Can Estimate the Gain with Half Branch



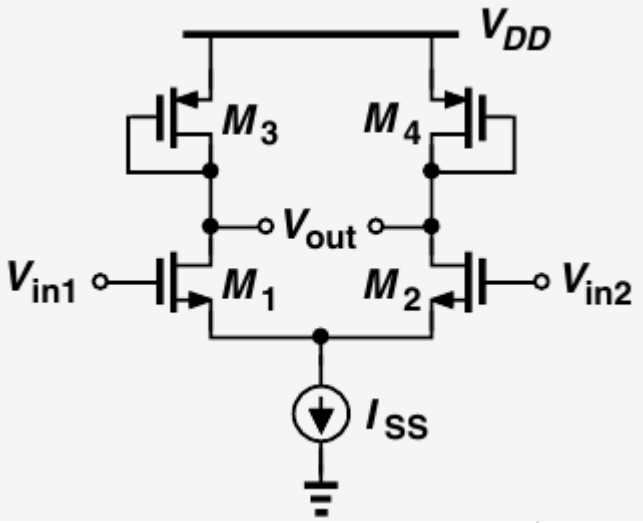
$$v_{out1} = -g_m R_D v_{in1}$$

$$v_{out2} = -g_m R_D v_{in2},$$

$$\frac{v_{out1} - v_{out2}}{v_{in1} - v_{in2}} = -g_m R_D.$$

Example 10.22

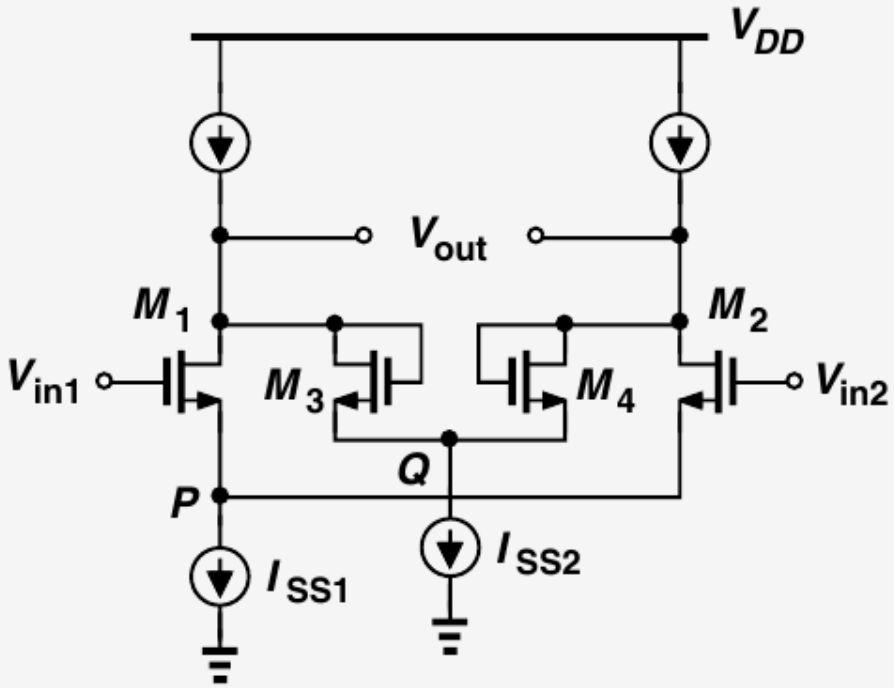
Determine the voltage gain of the circuit shown in Fig. 10.34(a). Assume $\lambda \neq 0$.



- Assume symmetry.

Example 10.23

Assuming $\lambda = 0$, compute the voltage gain of the circuit illustrated in Fig. 10.35(a).



(a)

Figure 10.35

Example 10.24

Assuming $\lambda = 0$, calculate the voltage gain of the topology shown in Fig. 10.36(a).

