Level Shifters

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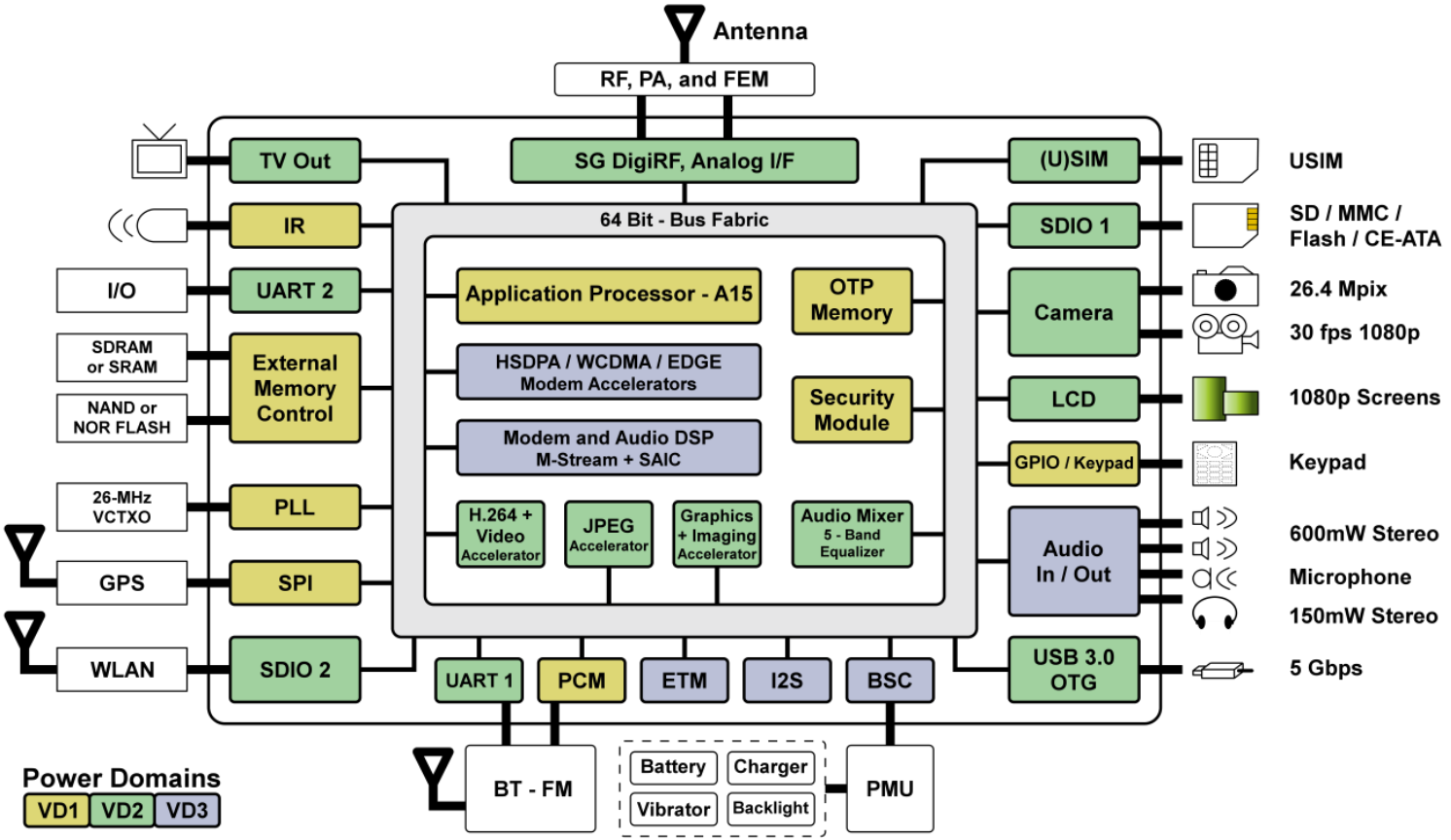
Contents

- Why do we use level shifters?
- Conventional level shifters and Issues
- Various level shifter structures

Why Do We Use Level Shifter?

- Multiple supply voltage domain can be used for various reasons such as energy efficiency maximization and noise immunity.

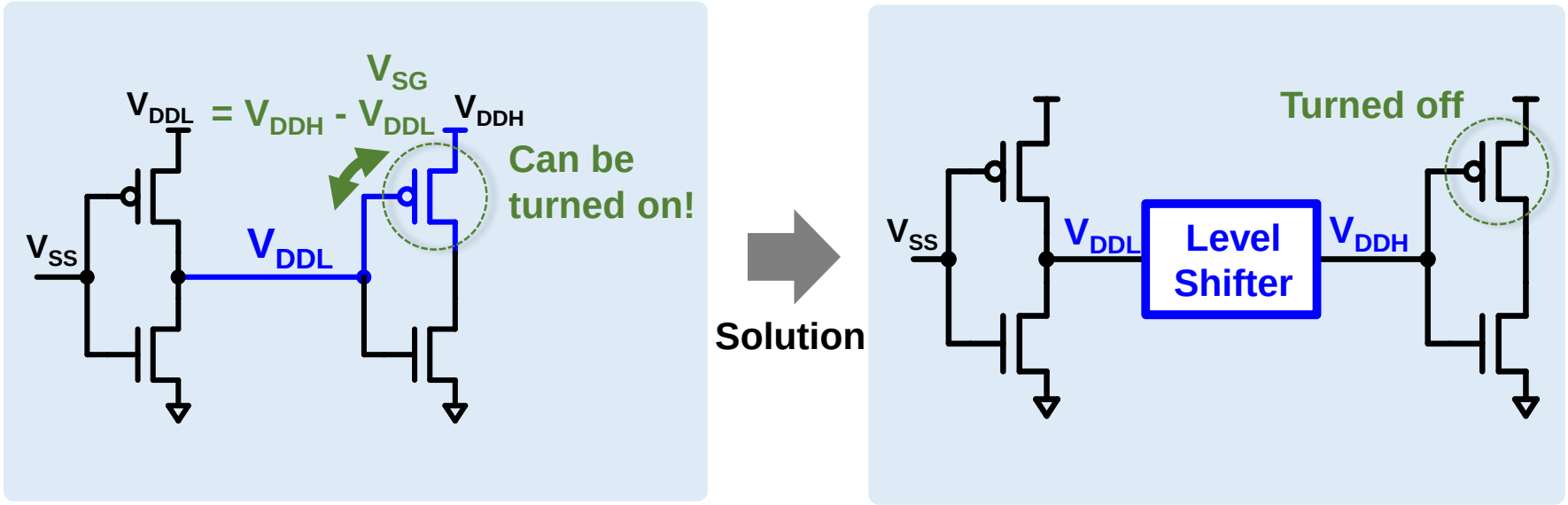


Necessity for Level Shifter (LS)

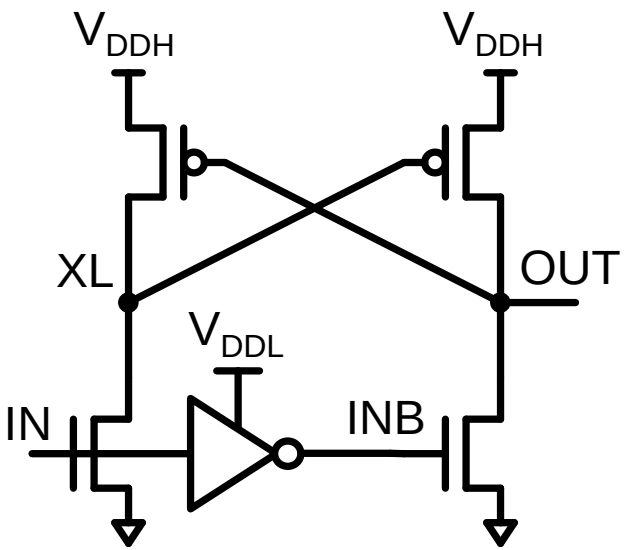
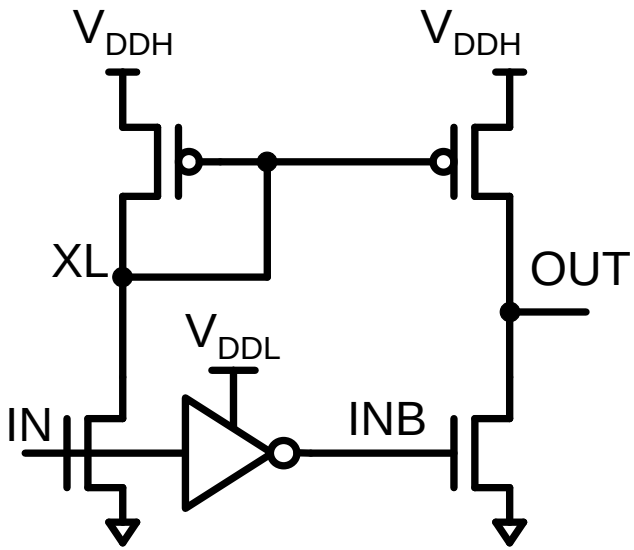
- Left bottom shows an inverter in the lower supply voltage domain (V_{DDL}) driving an inverter in the higher supply voltage domain (V_{DDH}).

  ➔ Even 1st stage inverter output is high, the pFET in the 2nd stage inverter can be turned on if $V_{DDH} - V_{DDL} > V_{th}$ and burn contention current.

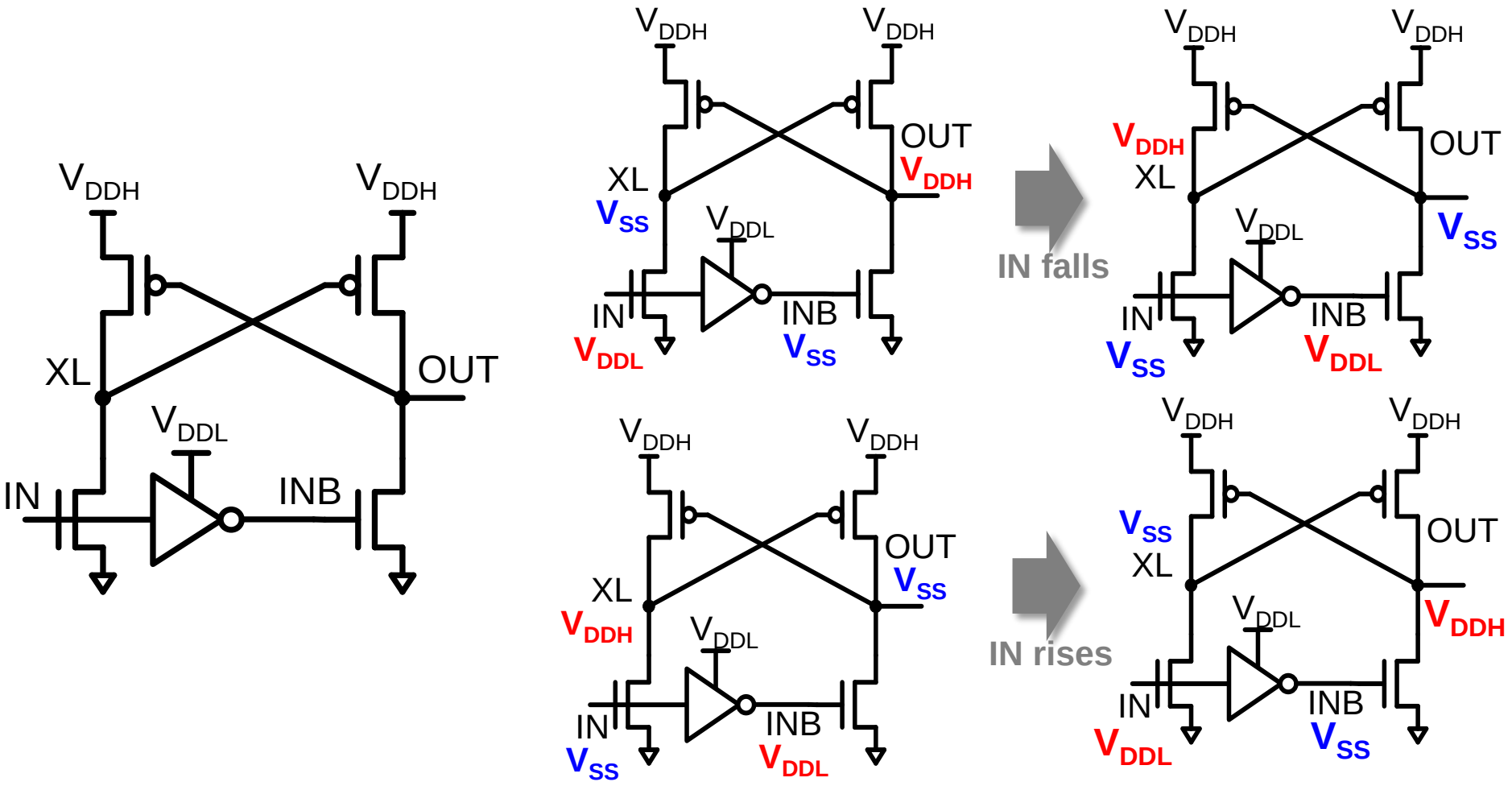
- To handle this problem in V_{DD} domain cross, a level shifter (LS) is required.



Conventional Level Shifter Structures

Cross-coupled PFET LS (CPLS)	Current mirror based LS (CMLS)
	

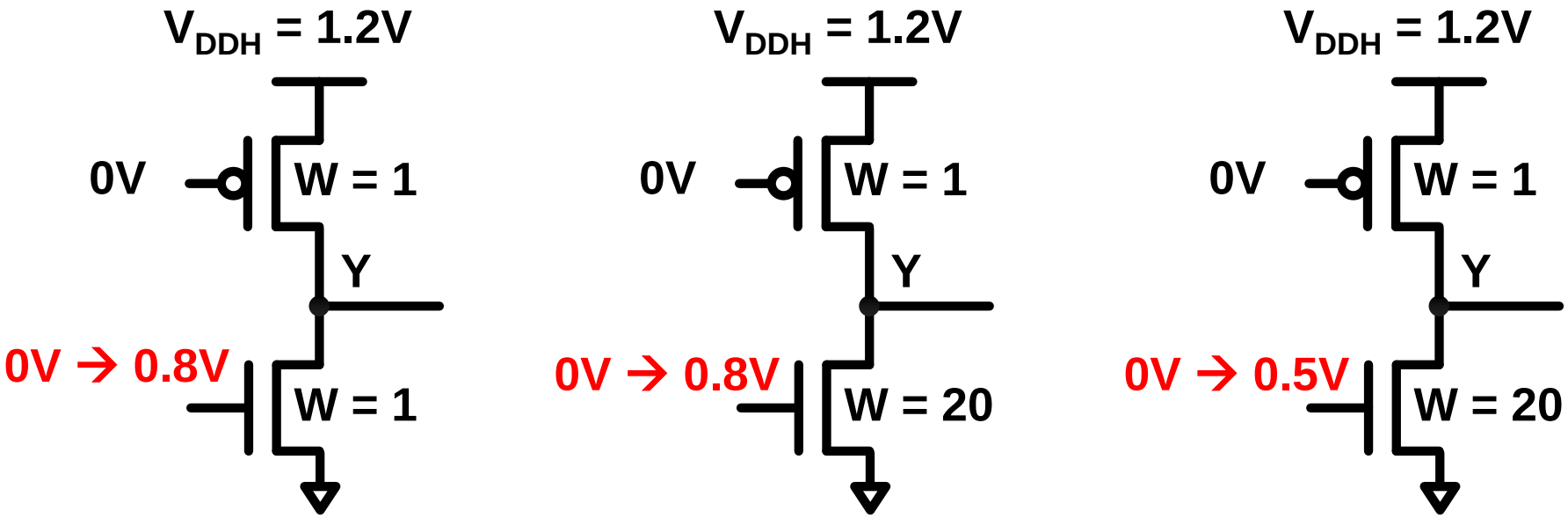
Revisit the Operation of CPLS



What if?
Voltage Lowering w/ Contention

- Consider the following case. Can Y be lowered?

➔ **Note that this is the key trigger of CPLS operation!**

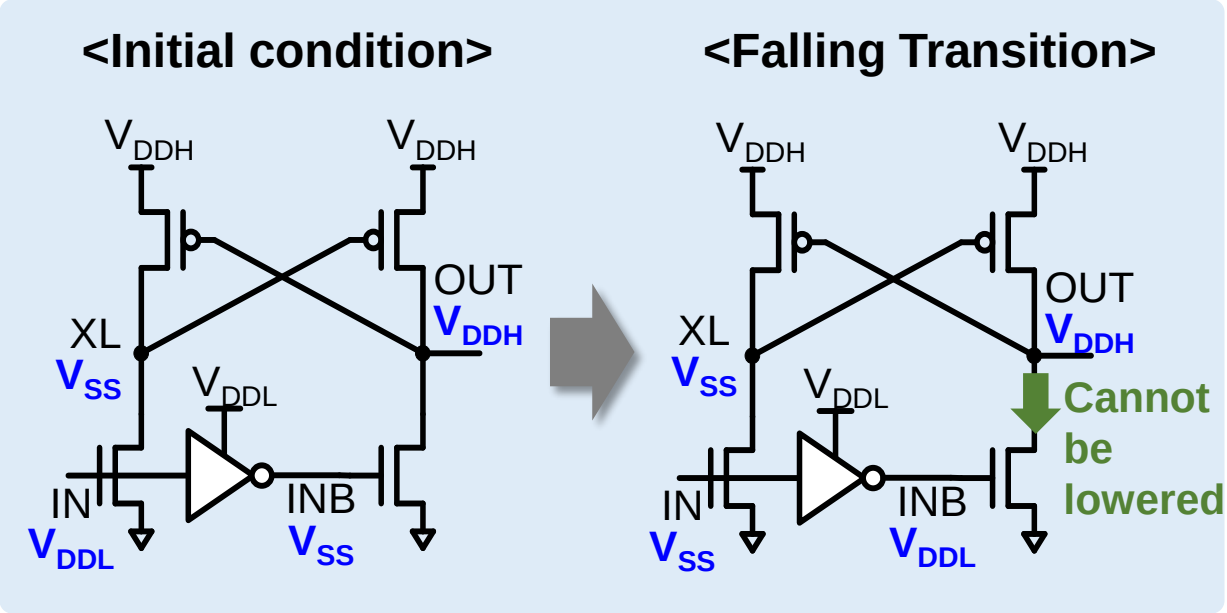


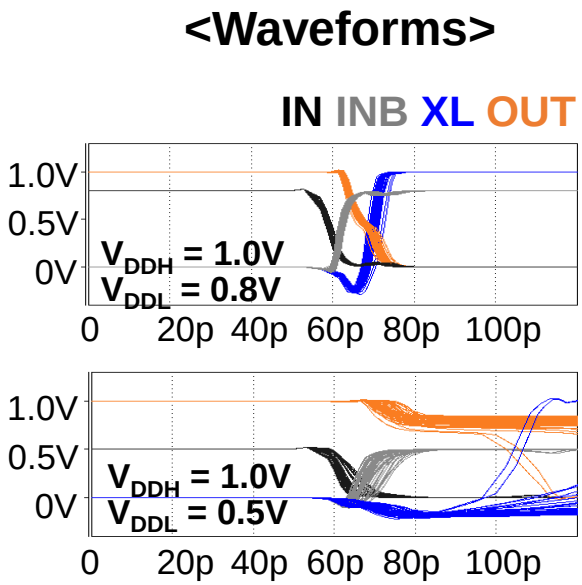
- It is desirable for an LS to operate not only when **V_{DDL} = 0.8V & V_{DDH} = 1.2V** but also **V_{DDL} = 0.5V & V_{DDH} = 1.2V**. (Wide range!)

Limitation of CPLS

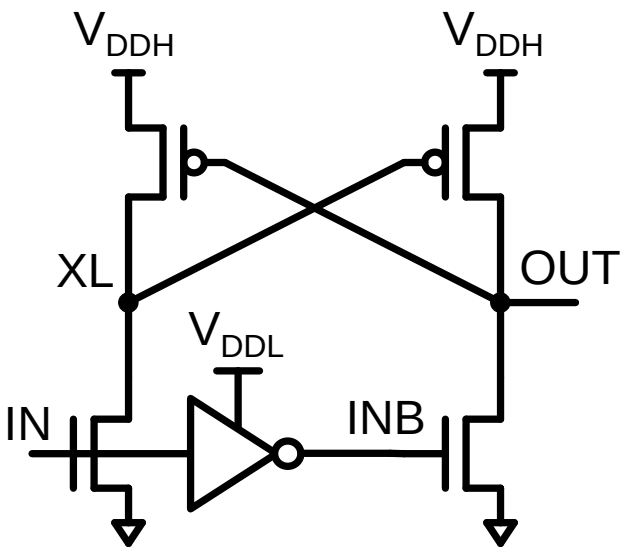
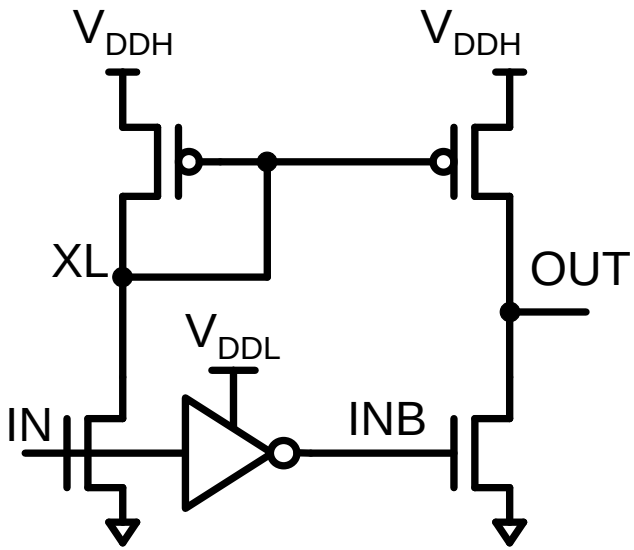
- Very strong (wide) nMOS are required to provide enough current to pull down XL or OUT to the ground, leading to increase in the delay, area and the power dissipation.

➔ **It is highly difficult to achieve wide range operation.**



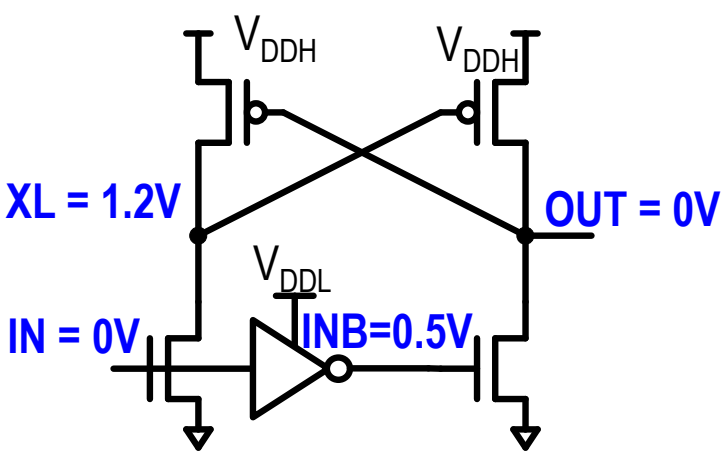
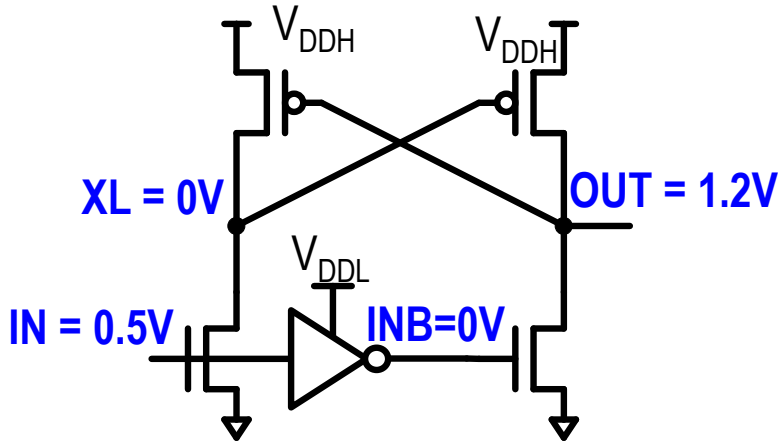
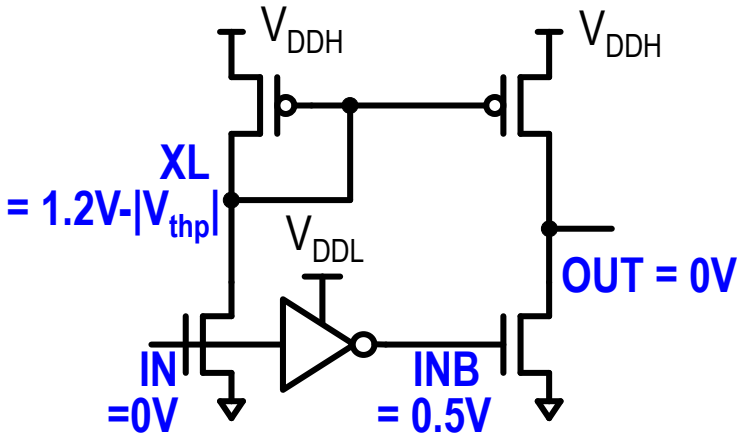
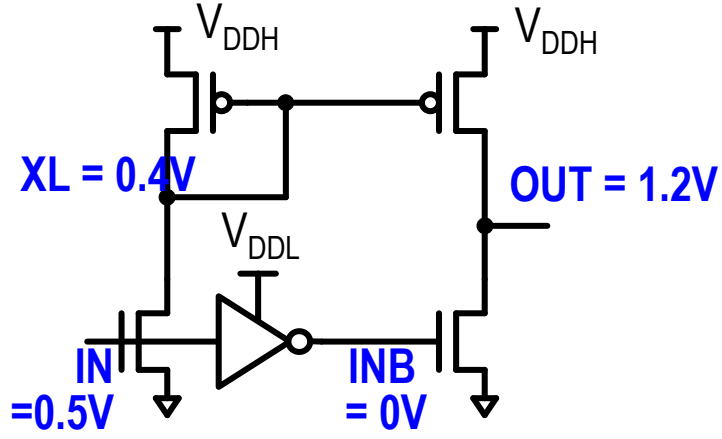


Revisit
Conventional Level Shifter Structures

Cross-coupled PFET LS (CPLS)	Current mirror based LS (CMLS)
	

See the Initial Condition of CMLS! Compared to CPLS

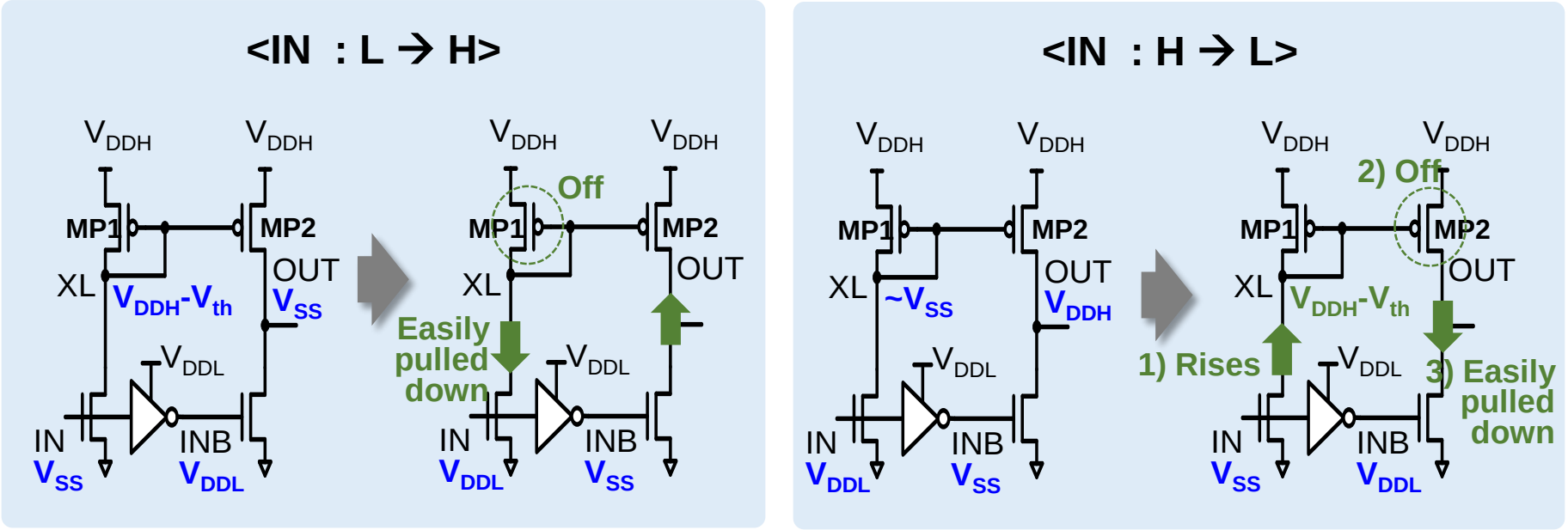
- Problem : Initially strongly turn-on pMOS cannot be overcome by nMOS!

	When IN = 0 and OUT = 0	When IN = 1 and OUT = 1
CPLS		
CMLS		

Contention-Free Operation of CMLS

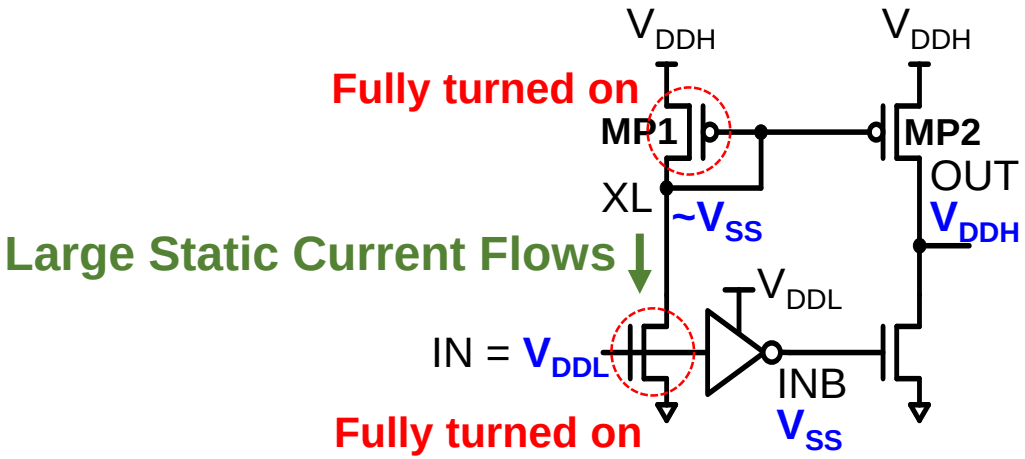
- CMLS is relatively free from the contention problem of CPLS.
  - When IN : L → H, XL can be easily lowered because the initial V_{SG} of MP1 is V_{th} (=MP1 is off), not V_{DDH} (=MP1 is fully turned on) as in CPLS.
  - When IN : H → L, OUT can be easily lowered because XL rises to $V_{DDH} - V_{th}$ as soon as IN is lowered, which weakens MP2.

➔ CMLS operates high speed without exceedingly large NMOS devices.



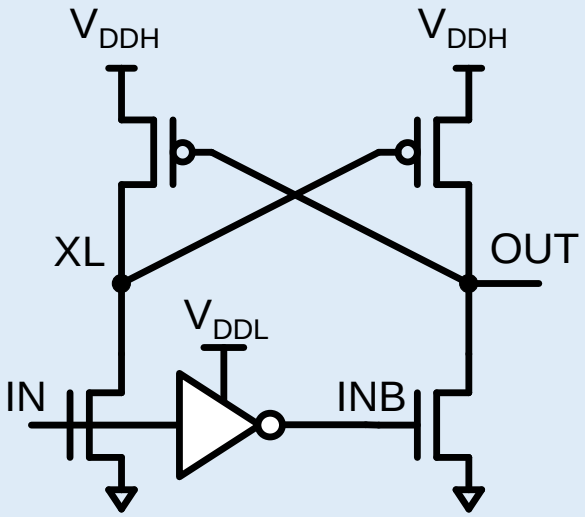
Limitation of CMLS

- When IN is stayed with V_{DDL} in CMLS, a large static current flows, which significantly increases power dissipation.



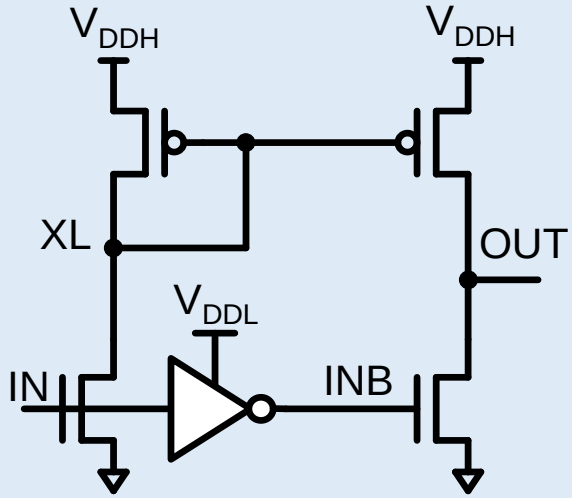
Key Design Consideration of LS

<CPLS>



✓ Wide range operation is unachievable in CPLS.

<CMLS>

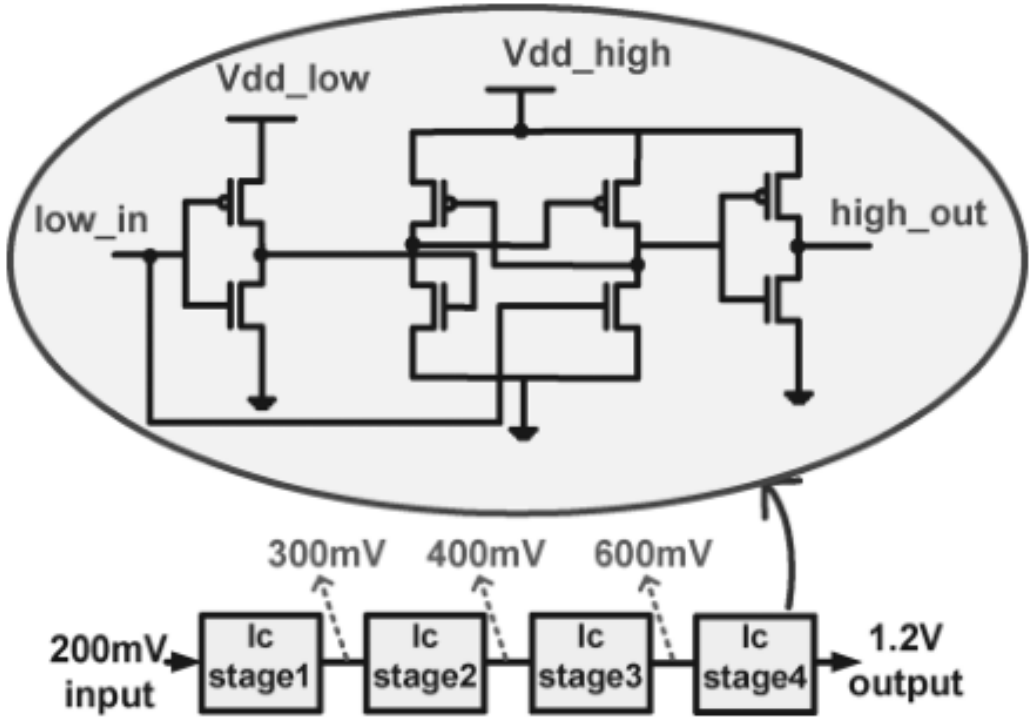


✓ Large power consumption due to static current.

➔ **Wide-range & energy efficient** level shifter design is required.

Ideation for CPLS ;Cascading CPLS

1) Single CPLS only can convert narrow range
2) How about cascading multiple CPLS?



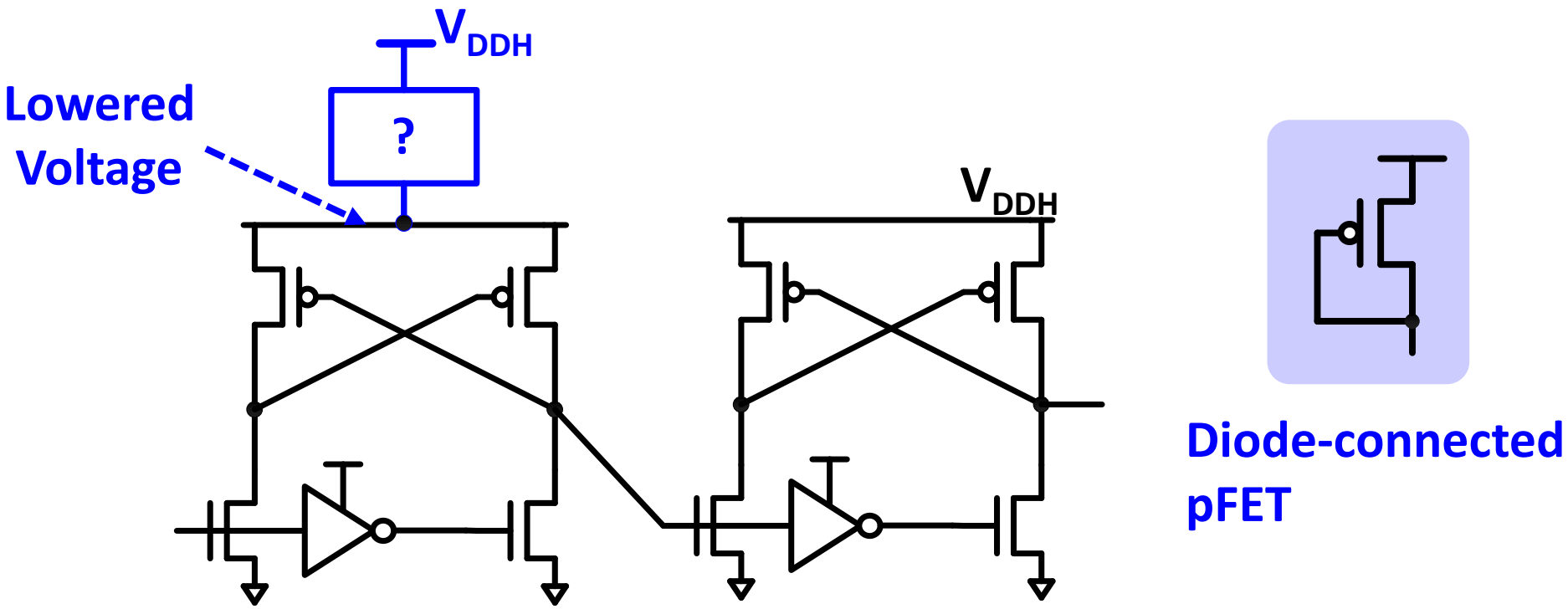
Limitations

- ✓ Generation of intermediate supply voltage incur power and area penalty.
- ✓ Limited speed performance due to multiple stage conversion.

B. Zhai, et al, "Energy-Efficient Subthreshold Processor Design," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 17, pp. 1127-1137, 2009.

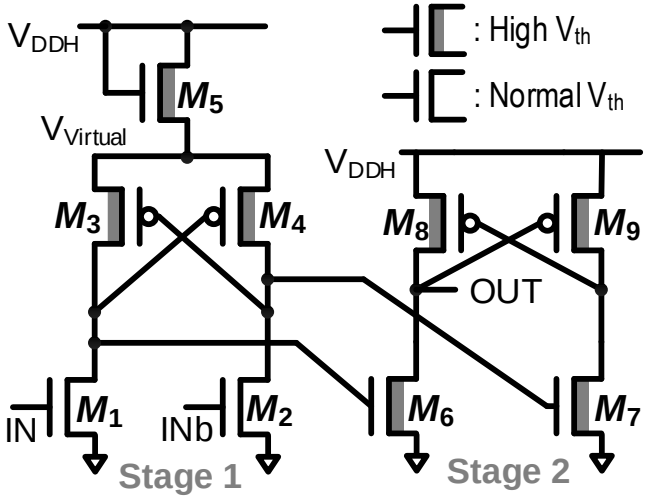
Ideation for CPLS ;Two Stage CPLS w/ Diode PFET Header

1) Generation of intermediate V_{DD} is very cumbersome.
2) Is there any simple way to generate intermediate V_{DD} while still using cascading CPLS? Then, we can implement it only with V_{DDH}.
3) How about using a simple diode-connected pFET? Like,



Two Stage CPLS w/ Diode PFET Header

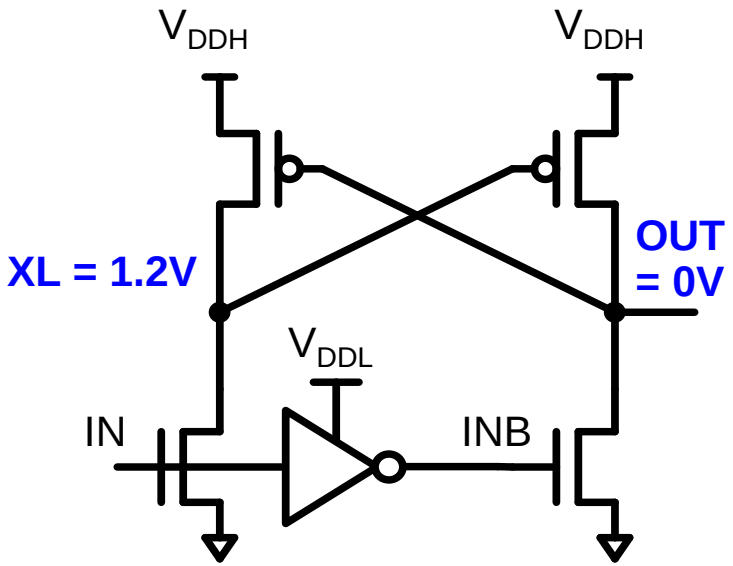
- **Goal**
  - Intermediate supply voltage is created with diode connected PMOS at 1st stage to weaken the pull-up strength of CPL.
  - Multi-threshold technology is used to further weaken the pull-up.
- **Limitations**
  - Speed degradation due to two stage operation
  - Use of multi-threshold technology is complex and expensive.

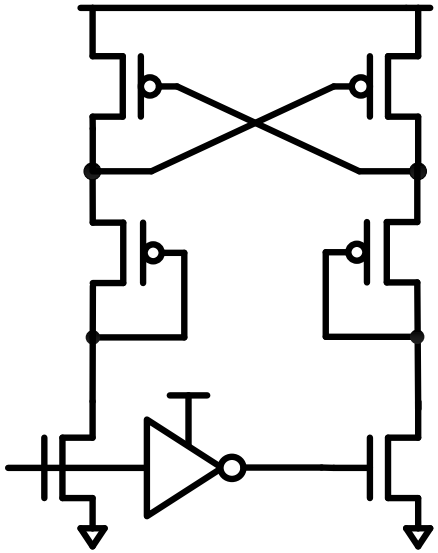


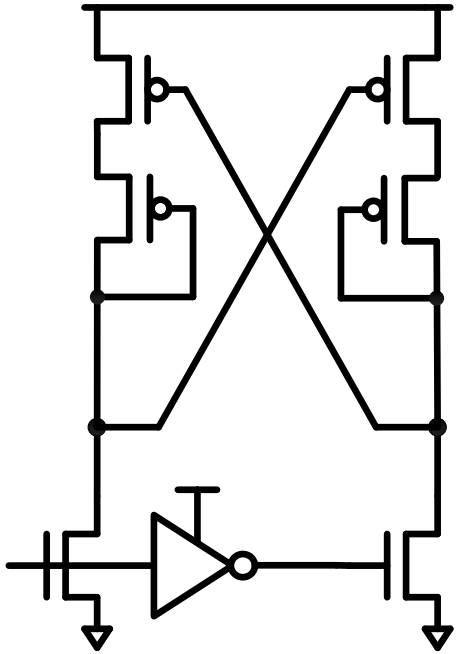
S. N. Wooters, et al," IEEE Transactions on *Circuits and Systems II: Express Briefs, IEEE Transactions on,* vol. 57, pp. 290-294, 2010.

Ideation for CPLS

1) Key limitation of CPLS is the contention b/w pMOS & nMOS
2) How can we mitigate the contention?
3) Can we make the pull-up path significantly weaker?

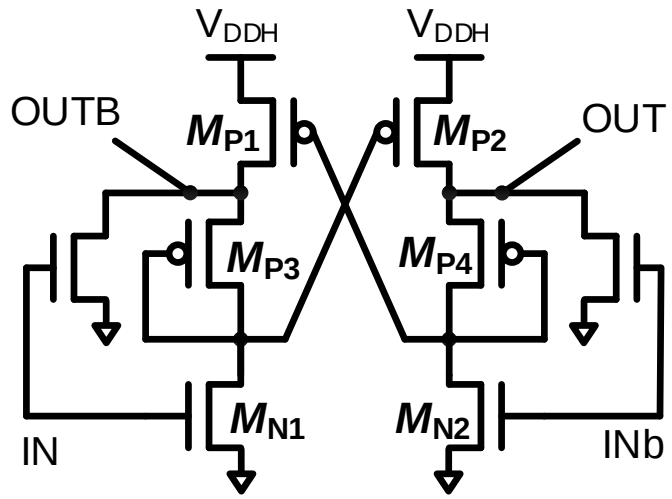






CPLS with Diode Connected PFET Insertion

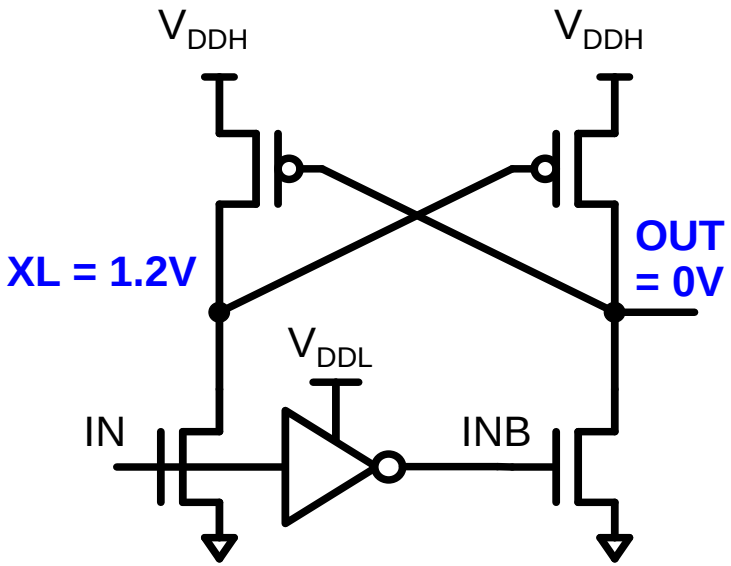
- **Goal**
  - Diode MP3 and MP4 are added to limit the pull-up strength.
  - MN3 and MN4 guarantee full swing of OUTBH and OUTH nodes.
- Limitations
  - Static current path of MP2 and MN4 when IN=low.

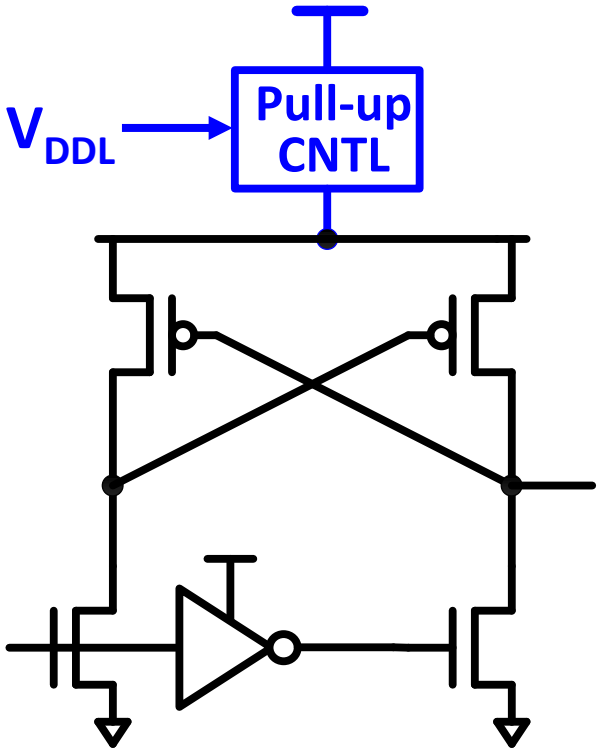


H. Shao and C.-Y. Tsui, "A robust, input voltage adaptive and low energy consumption level converter for sub-threshold logic," in Proc. 33rd *ESSCIRC*, Sep. 2007, pp. 312–315.

Ideation for CPLS

1) Key limitation of CPLS is the contention b/w pMOS & nMOS
2) Can we make the pull-up path significantly weaker?
3) More effectively, only when V_{DDL} is small!

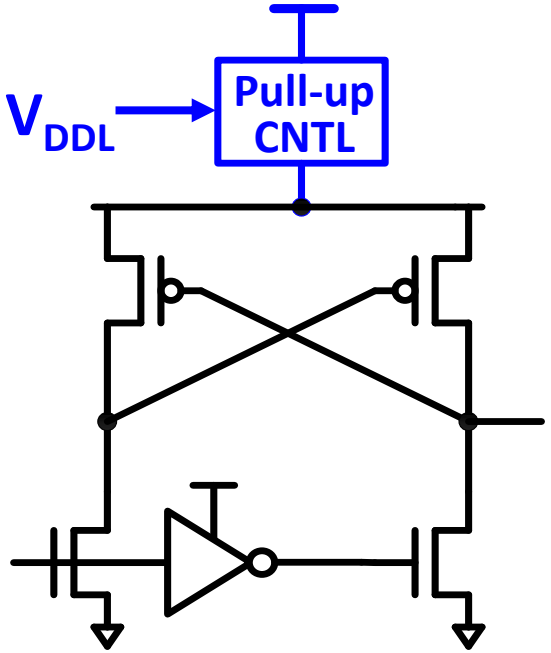




How Can We Control Pull-up Strength w/ V_{DDL}?

- Express your aim verbally!

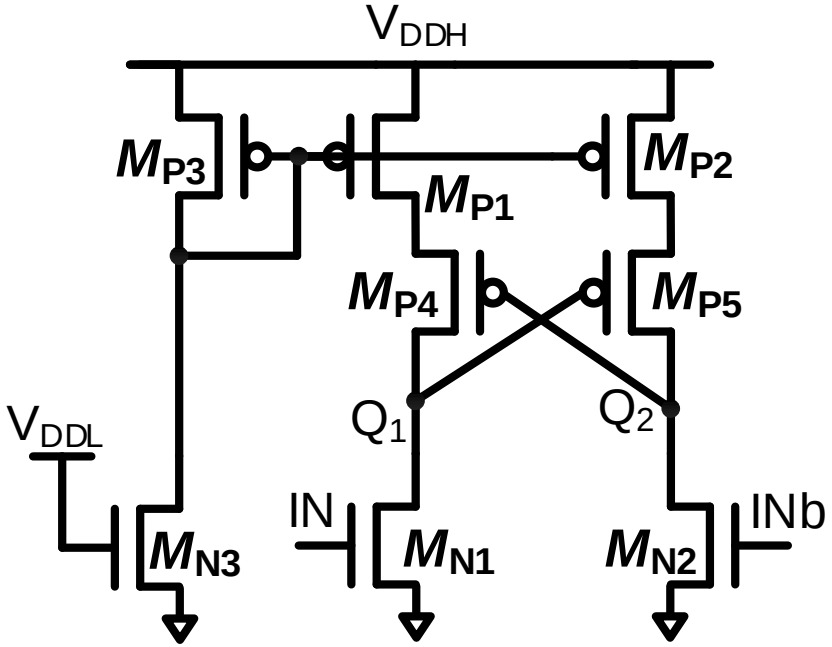
➔ **When V_{DDL} is lower, pull-up should be weaker.**



- **Another conclusion: with nMOS + pull-up pMOS current mirror, we can control pull-up network with V_{DDL}.**

LS with Current Limiter

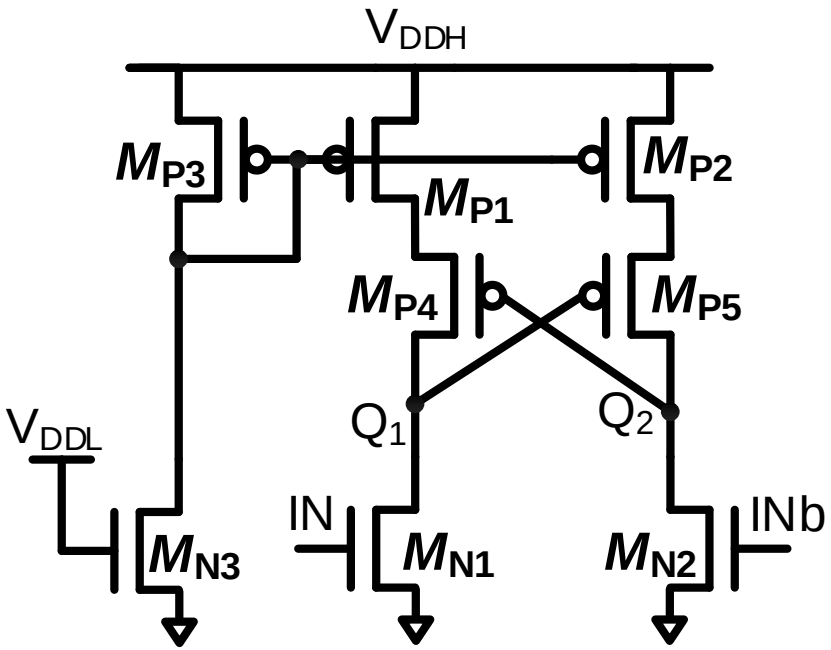
- **Goal**
  - Reducing the drive strength of pull-up network in CPLS by biasing M_{P1} and M_{P2} with intermediate voltage.
- **Limitations**
  - Static current in the bias voltage generation circuit.

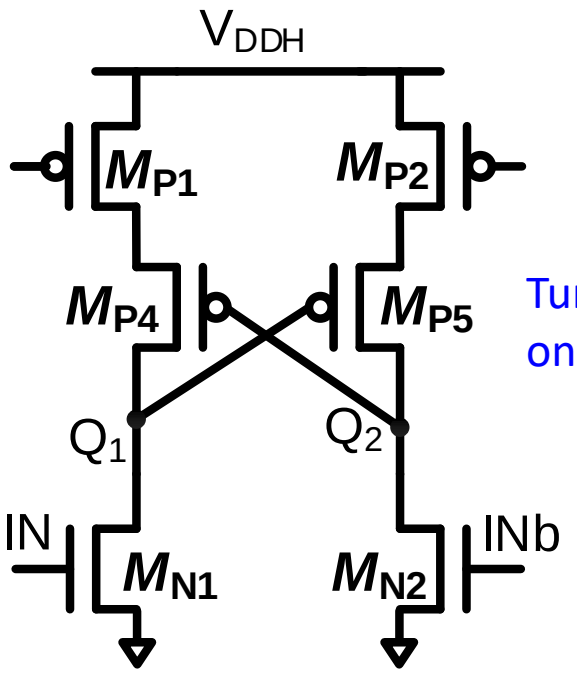


T.-H. Chen, J. Chen, and L. T. Clark, "Subthreshold to above threshold level shifter design," J. Low Power Electron., vol. 2, no. 2, pp. 251–258, August 2006

Ideation for Current Limiter CPLS

1) Static current is wasted.
2) Can we make the pull-up controller is only turned on only **when/where** it is required?





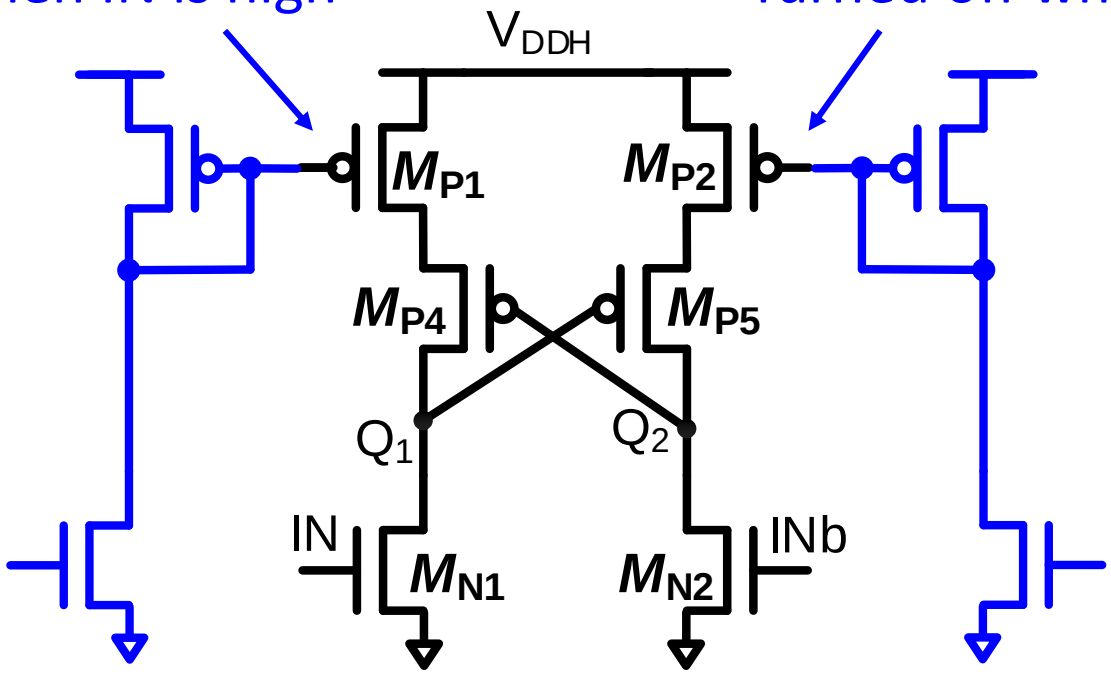
Turning on MP1 and MP2 only when they are required.

How Can We Adaptively Control Pull-up Network?

- **Focus on "where"**

Turned on when IN is low
Turned off when IN is high

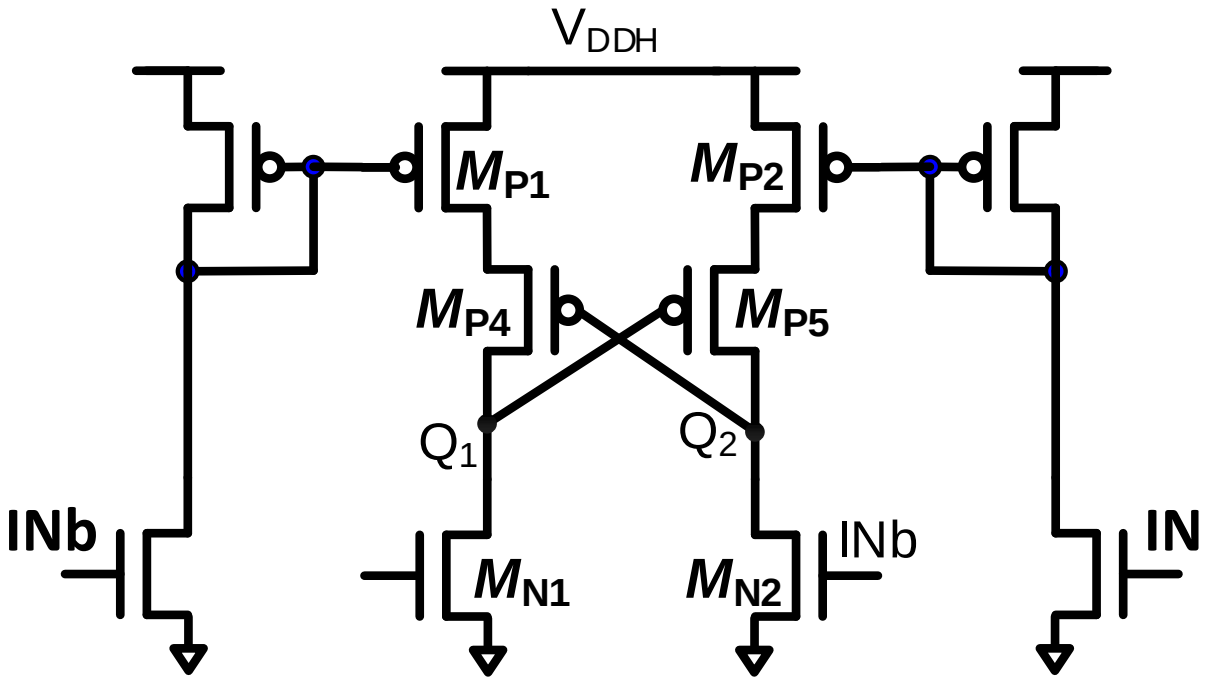
Turned on when INb is low
Turned off when INb is high



How Can We Block the Static Current?

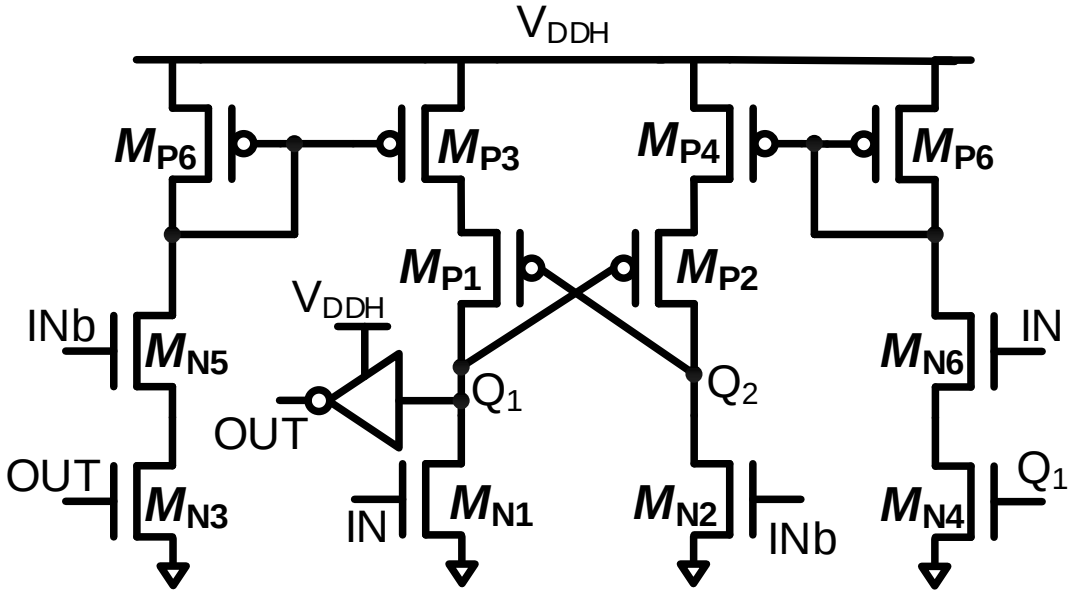
- Still **“when”** should be addressed!
- After the transition finishes, MP1 and MP2 should be turned off back.

➔ How can we detect whether the transition is finished?



Adaptive Current Limiter CPLS

- **Goal**
  - IN and OUT are compared to selectively supply the current to the path to be pulled up.
- **Limitations**
  - When IN=0, Q1 retains with float high, which makes vulnerable to noise.

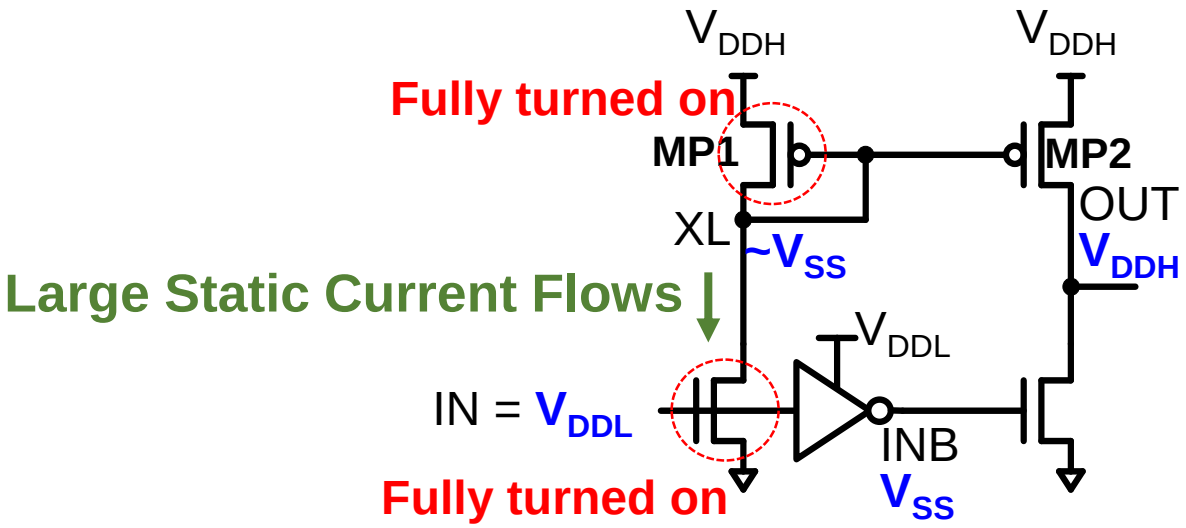


S. R. Hosseini, et al., "A Low-Power Subthreshold to Above-Threshold Voltage Level Shifter," *Circuits and Systems II: Express Briefs, IEEE Transactions on,* vol. 61, pp. 753-757, 2014.

Ideation for CMLS

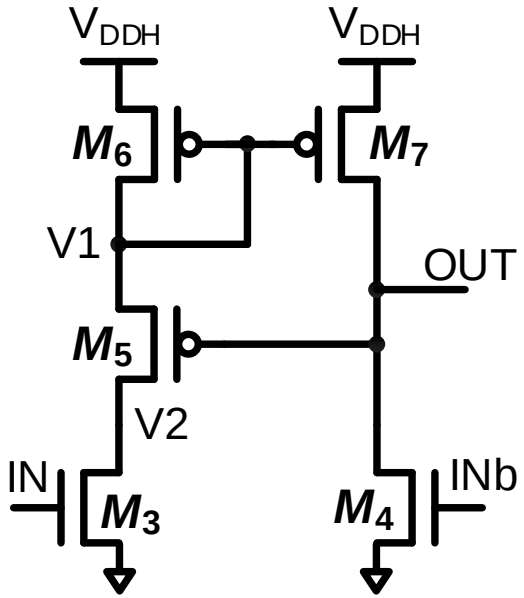
1) Key limitation of CMLS is the static current when IN is high
2) Can we make block the short-circuit current after the transition finishes?

➔ **How can we detect whether the transition is finished?**



Wilson's Current Mirror Level Shifter

- **Goal**
  - Static current in CMLS is removed by feedback pMOS M5.
- **Limitations**
  - Rising time and rising level of output node (Z) is greatly degraded because V1 cannot be decreased sufficiently due to M5.
  - Out is float high when IN is high



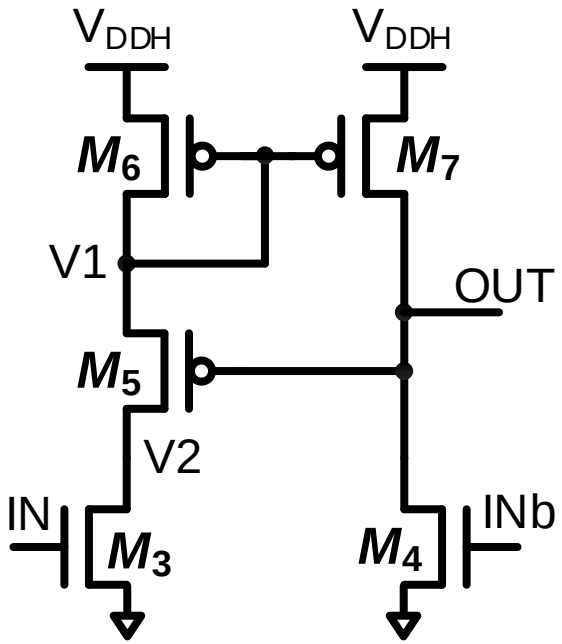
Lu, x, S. tkemeier, and U. Ruckert, "A Subthreshold to Above-Threshold Level Shifter Comprising a Wilson Current Mirror," *Circuits and Systems II: Express Briefs, IEEE Transactions on,* vol. 57, pp. 721-724, 2010.

Ideation for Improving Wilson's CMLS

1) One problem is the rising performance of output node (Z) is greatly increased because V1 cannot be decreased sufficiently due to M5.

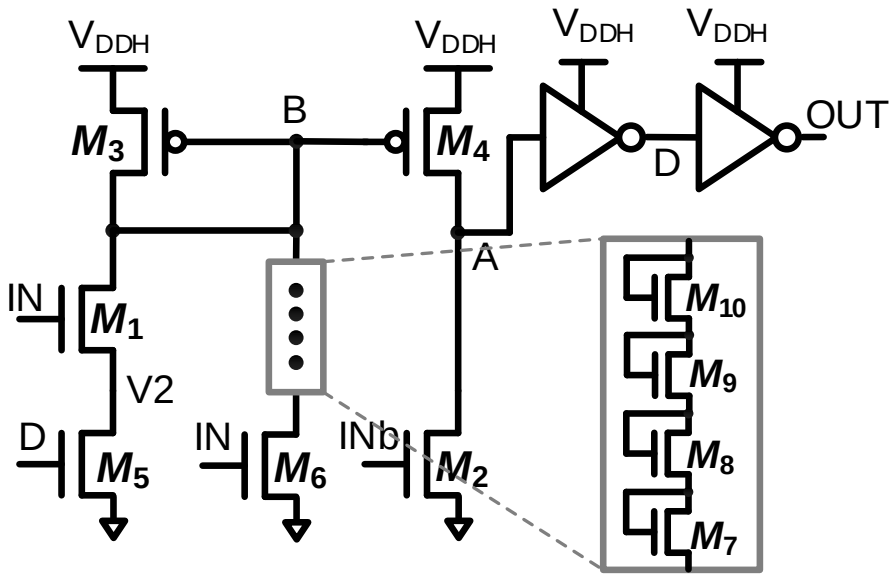
➔ Can we delay the turn-off moment of M5 a little bit?

2) Another problem is OUT is floated high. ➔ Can we keep V1 low for high IN?



CMLS With Diode Chain

- **Goal**
  - Speed degradation and floating OUT problem in WCMLS are resolved
- **Limitations**
  - Trade-off between the static current vs. noise stability



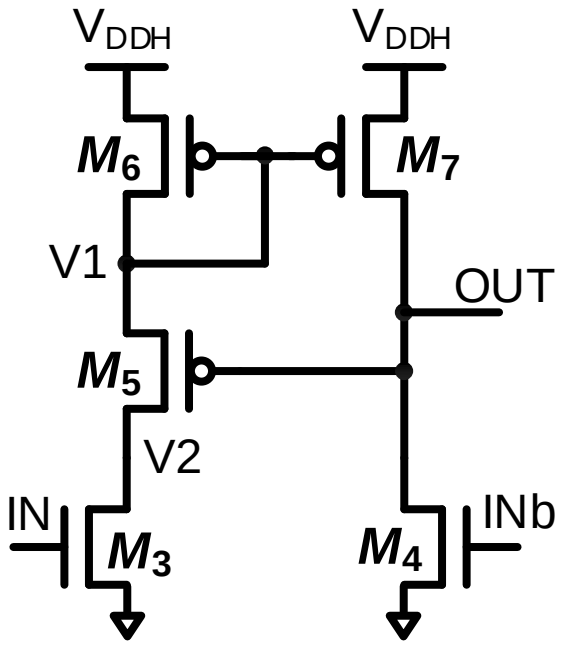
J. Zhou et al, "An Ultra-Low Voltage Level Shifter Using Revised Wilson Current Mirror for Fast and EnergyEfficient Wide-Range Voltage Conversion from Sub-Threshold to I/O Voltage," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 62, no. 3, pp. 697-706, 2015.

Ideation for Improving Wilson's CMLS

1) One problem is the rising performance of output node (Z) is greatly increased because V1 cannot be decreased sufficiently due to M5.

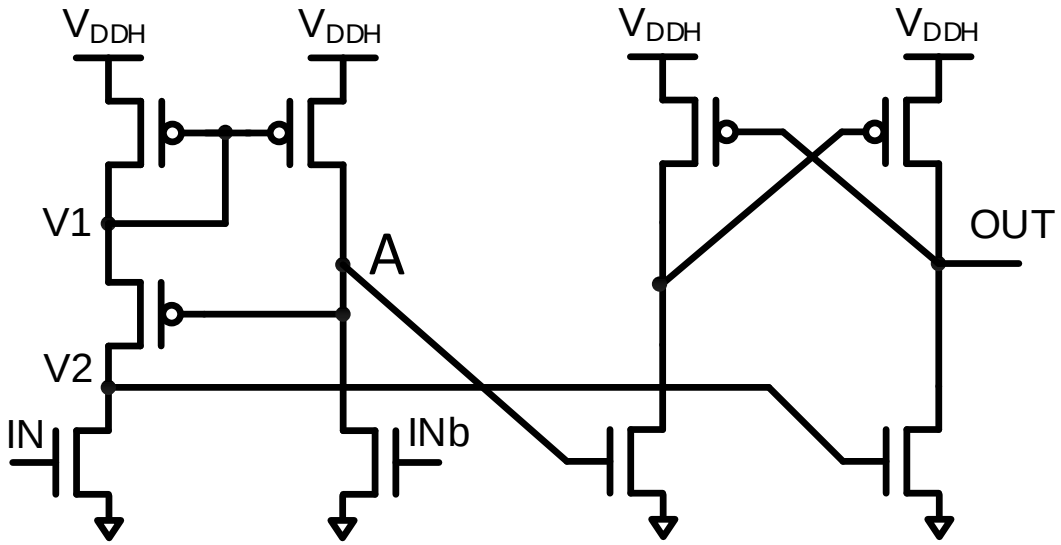
➔ This means that OUT becomes only 0.9V… while it should be 1.2V.

➔ Can we amplify the OUT?



CMLS + CPLS

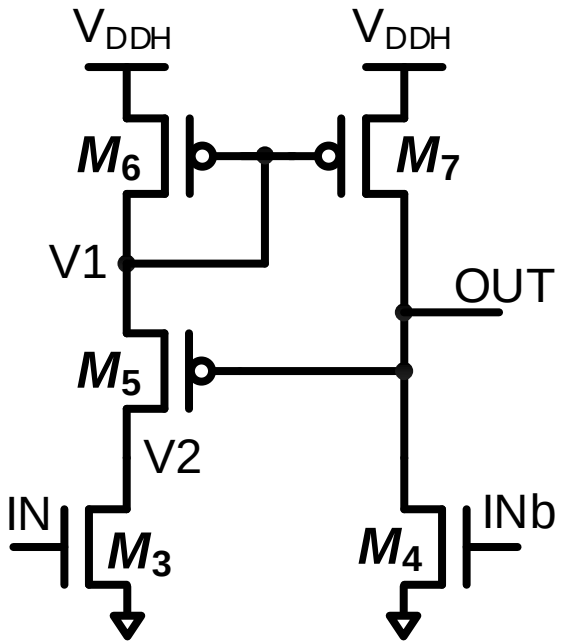
- **Goal**
  - Speed degradation of OUT problem in WCMLS are resolved
- **Limitations**
  - The node A is still floated high.
  - Two stage operation limits the overall speed

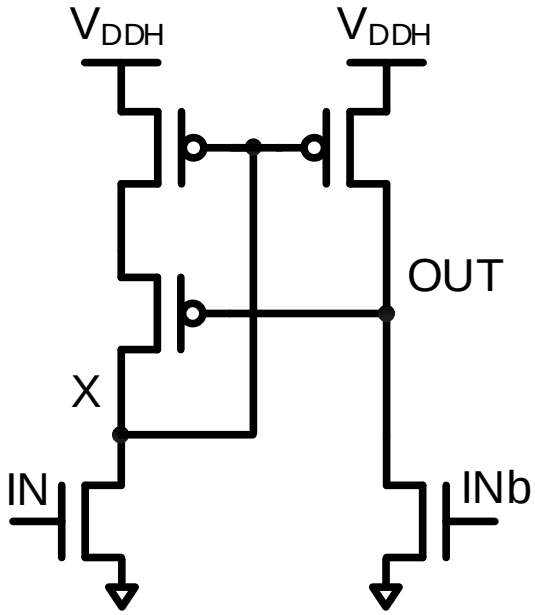


Y. Cao, et al, "A Compact 31.47 fJ/Conversion Subthreshold Level Shifter With Wide Conversion Range in 65 nm MTCMOS," in *IEEE Access*, vol. 6, pp. 54976-54981, 2018

Ideation for Improving Wilson's CMLS

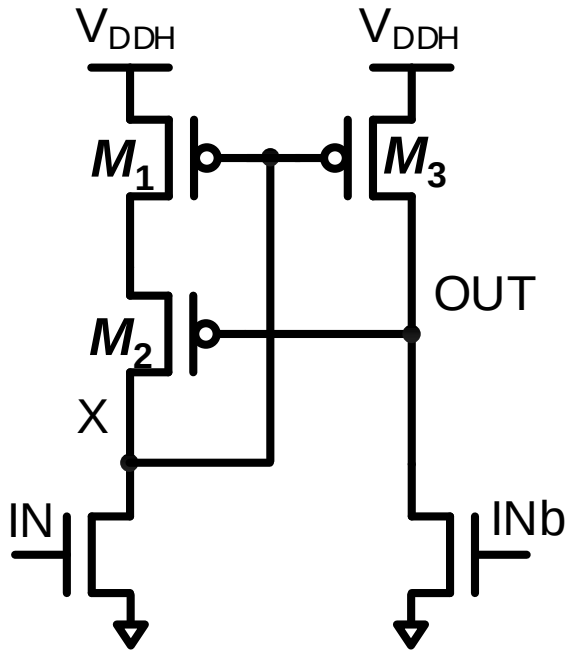
1) How about making V1 fall to full 0? Then we can achieve high speed OUT rising and OUT will not be floated.
2) By how?





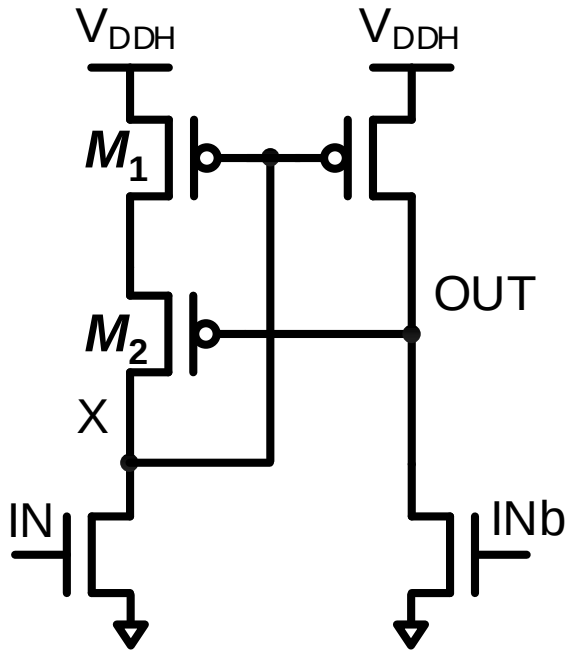
Operation Verification For Rising

- When IN = 0 ➔ 1,
  1) OUT would be initially low, and X would be $V_{DDH} - |V_{thp}|$
  2) Although M2 is turned on, X can be easily pulled down, because M1 is initially off.
  3) Lowered X pulls up OUT, leading to turn off M2. Thus, X can be fully pulled-down to zero.
  4) OUT can be raised quickly and be driven full VDD without floating



Operation Verification For Falling

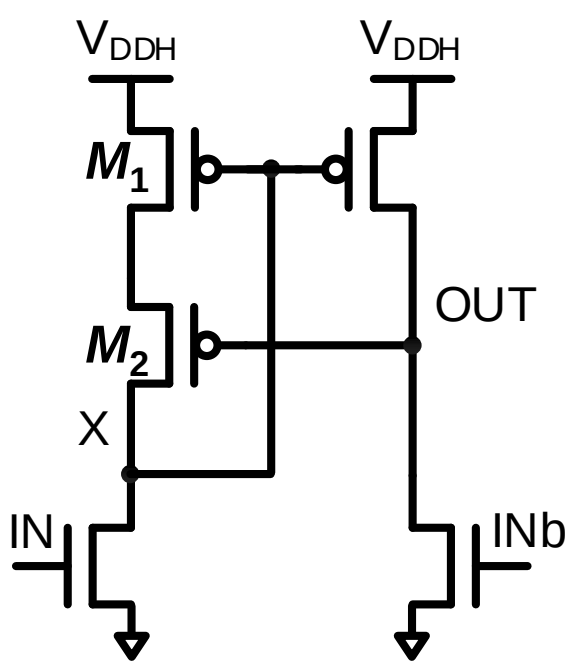
- When IN = 1 ➔ 0, (INb = 0→1)
  1) OUT would be initially high, and X is initially 0V.
  2) Although OUT should be pulled down by rising INb, the contention prevents OUT from falling.
  3) Thus, level shifting may not occur (**malfunction**).

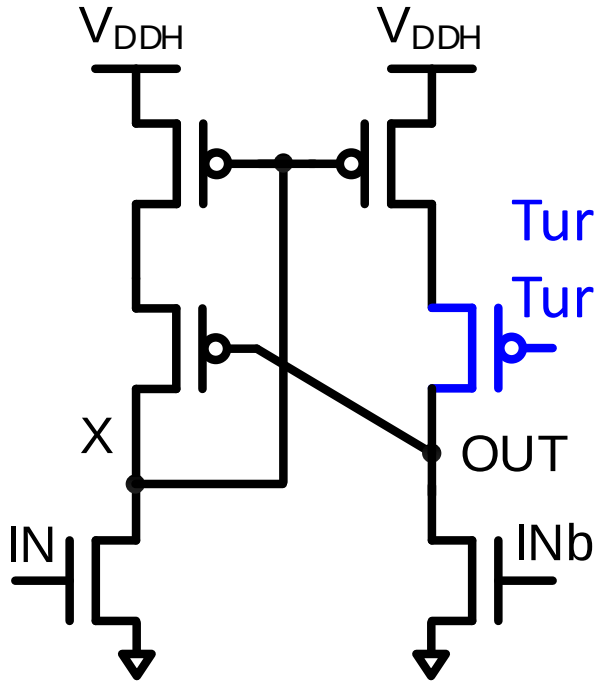


➔ **How can we solve this?**

Just Focus on the Problem! Ideation!

1) When IN = 1 ➔ 0, (INb = 0→1), OUT should be lowered.
2) Pull-up path can be blocked for the above case.
3) How can we implement it? ➔ **Express it verbally!**





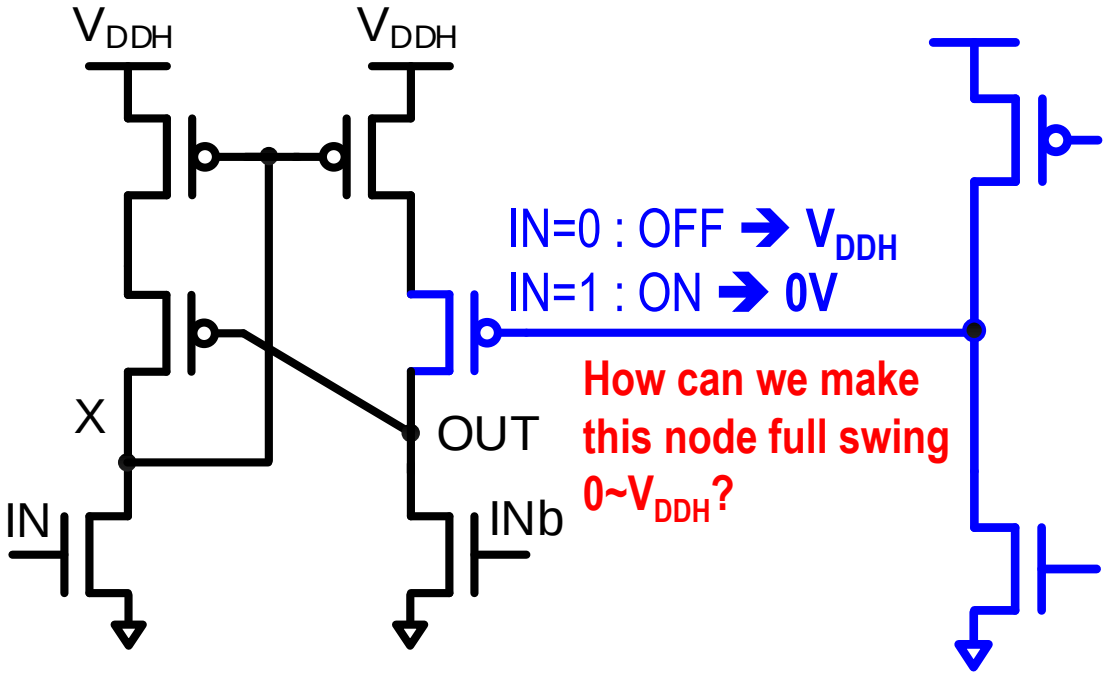
Turns off when IN=0 & INb = 1
Turns on when IN=1 & INb = 0

How to Realize Through Circuit

1) We need ON & OFF; pMOS and nMOS both are required.
2) Can we directly connect IN? ➔ **No! (Why?)**
3) How can we make the circuit controlled by V_{DDL} swing signal?

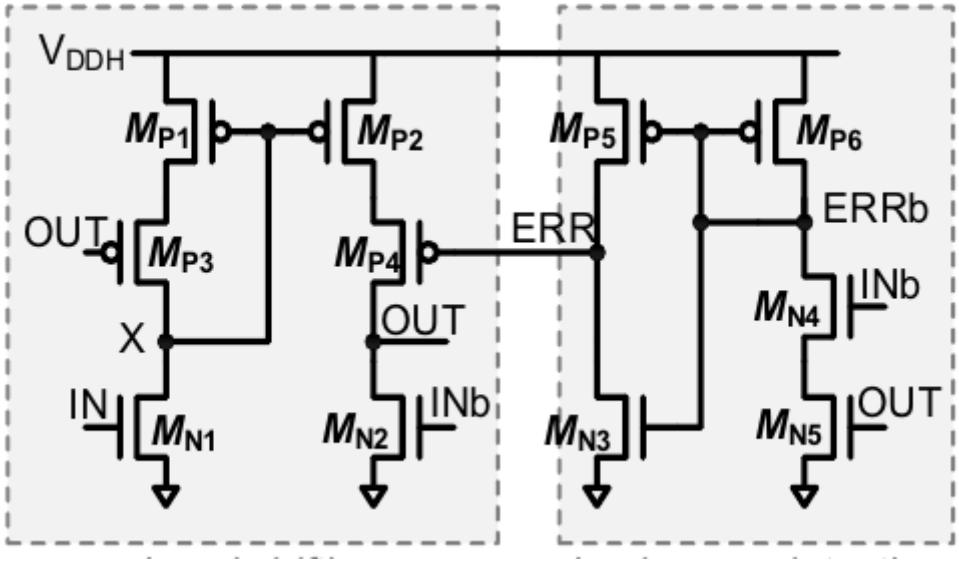
➔**nMOS + pMOS current Mirror; but swing of the output is limited**

➔**We can utilize the restoring feature of the inverter!**



Static Current Free CMLS w/ LECC

- Logic error detection circuit is employed to control M4



H. Jeong, et al. "A Wide-Range Static Current-Free Current Mirror-Based LS With Logic Error Detection for Near-Threshold Operation." *IEEE Journal of Solid-State Circuits*, 2020.

Summary

- Level shifter is required to stably transfer the signal across different VDD domain.
- The conventional level shifters have two main limitations; CPLS has limited voltage range while CMLS consumes large static power.
- In order to resolve the limitations of the conventional LSs, there are many level shifters proposed.
- We saw the step by step ideation procedure for each level shifter development.