Level Shifters

Hanwool Jeong
hwjeong@kw.ac.kr
Contents

• Why do we use level shifters?
• Conventional level shifters and Issues
• Various level shifter structures
Multiple supply voltage domain can be used for various reasons such as energy efficiency maximization and noise immunity.
Necessity for Level Shifter (LS)

- Left bottom shows an inverter in the lower supply voltage domain ($V_{DDL}$) driving an inverter in the higher supply voltage domain ($V_{DDH}$).

  ➔ Even 1$^{st}$ stage inverter output is high, the pFET in the 2$^{nd}$ stage inverter can be turned on if $V_{DDH} - V_{DDL} > V_{th}$ and burn contention current.

- To handle this problem in $V_{DD}$ domain cross, a level shifter (LS) is required.
Conventional Level Shifter Structures

<table>
<thead>
<tr>
<th>Cross-coupled PFET LS (CPLS)</th>
<th>Current mirror based LS (CMLS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DDH}$</td>
<td>$V_{DDH}$</td>
</tr>
<tr>
<td>$V_{DDL}$</td>
<td>$V_{DDL}$</td>
</tr>
<tr>
<td>$XL$</td>
<td>$XL$</td>
</tr>
<tr>
<td>$IN$</td>
<td>$IN$</td>
</tr>
<tr>
<td>$INB$</td>
<td>$INB$</td>
</tr>
<tr>
<td>$OUT$</td>
<td>$OUT$</td>
</tr>
<tr>
<td>$V_{DDH}$</td>
<td>$V_{DDH}$</td>
</tr>
<tr>
<td>$V_{DDL}$</td>
<td>$V_{DDL}$</td>
</tr>
<tr>
<td>$XL$</td>
<td>$XL$</td>
</tr>
<tr>
<td>$IN$</td>
<td>$IN$</td>
</tr>
<tr>
<td>$INB$</td>
<td>$INB$</td>
</tr>
<tr>
<td>$OUT$</td>
<td>$OUT$</td>
</tr>
</tbody>
</table>
Revisit the Operation of CPLS
What if?
Voltage Lowering w/ Contention

• Consider the following case. Can Y be lowered?

⇒ Note that this is the key trigger of CPLS operation!

• It is desirable for an LS to operate not only when $V_{DDL} = 0.8V$ & $V_{DDH} = 1.2V$ but also $V_{DDL} = 0.5V$ & $V_{DDH} = 1.2V$. (Wide range!)
Limitation of CPLS

- Very strong (wide) nMOS are required to provide enough current to pull down XL or OUT to the ground, leading to increase in the delay, area and the power dissipation.

⇒ It is highly difficult to achieve wide range operation.
Revisit
Conventional Level Shifter Structures

<table>
<thead>
<tr>
<th>Cross-coupled PFET LS (CPLS)</th>
<th>Current mirror based LS (CMLS)</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1" alt="CPLS Diagram" /></td>
<td><img src="image2" alt="CMLS Diagram" /></td>
</tr>
</tbody>
</table>

Symbols:
- **V_{DDH}**: Power Supply
- **V_{DDL}**: Differential Voltage
- **IN**: Input
- **INB**: Inverted Input
- **OUT**: Output
- **XL**: Cross-coupled Node
See the Initial Condition of CMLS! Compared to CPLS

- Problem: Initially strongly turn-on pMOS cannot be overcome by nMOS!

<table>
<thead>
<tr>
<th></th>
<th>When IN = 0 and OUT = 0</th>
<th>When IN = 1 and OUT = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPLS</td>
<td><img src="https://via.placeholder.com/150" alt="Diagram" /></td>
<td><img src="https://via.placeholder.com/150" alt="Diagram" /></td>
</tr>
<tr>
<td>XL = 1.2V</td>
<td>OUT = 0V</td>
<td>XL = 0V</td>
</tr>
<tr>
<td>IN = 0V</td>
<td>INB=0.5V</td>
<td>IN = 0.5V</td>
</tr>
<tr>
<td></td>
<td>OUT = 0V</td>
<td>OUT = 1.2V</td>
</tr>
<tr>
<td>CMLS</td>
<td><img src="https://via.placeholder.com/150" alt="Diagram" /></td>
<td><img src="https://via.placeholder.com/150" alt="Diagram" /></td>
</tr>
<tr>
<td>XL = 1.2V -</td>
<td>OUT = 0V</td>
<td>XL = 0.4V</td>
</tr>
<tr>
<td></td>
<td>IN = 0V</td>
<td>IN = 0.5V</td>
</tr>
<tr>
<td></td>
<td>OUT = 0V</td>
<td>OUT = 1.2V</td>
</tr>
</tbody>
</table>

\[ \Delta V \approx V_{DDH} \]
Contention-Free Operation of CMLS

- CMLS is relatively free from the contention problem of CPLS.
  - When \( \text{IN} \rightarrow \text{H} \), \( \text{XL} \) can be easily lowered because the initial \( V_{SG} \) of \( \text{MP1} \) is \( V_{th} \) (=MP1 is off), not \( V_{DDH} \) (=MP1 is fully turned on) as in CPLS.
  - When \( \text{IN} \rightarrow \text{L} \), \( \text{OUT} \) can be easily lowered because \( \text{XL} \) rises to \( V_{DDH} - V_{th} \) as soon as \( \text{IN} \) is lowered, which weakens \( \text{MP2} \).

→ CMLS operates high speed without exceedingly large NMOS devices.
Limitation of CMLS

- When IN is stayed with $V_{DDL}$ in CMLS, a large static current flows, which significantly increases power dissipation.
Key Design Consideration of LS

- Wide range & energy efficient level shifter design is required.

- Wide range operation is unachievable in CPLS.

- Large power consumption due to static current.

→ Wide-range & energy efficient level shifter design is required.
Ideation for CPLS; Cascading CPLS

1) Single CPLS only can convert narrow range
2) How about cascading multiple CPLS?

Limitations
✓ Generation of intermediate supply voltage incur power and area penalty.
✓ Limited speed performance due to multiple stage conversion.

Ideation for CPLS

1) Generation of intermediate $V_{DD}$ is very cumbersome.
2) Is there any simple way to generate intermediate $V_{DD}$ while still using cascading CPLS? Then, we can implement it only with $V_{DDH}$.
3) How about using a simple diode-connected pFET? Like,
Two Stage CPLS w/ Diode PFET Header

• **Goal**
  - Intermediate supply voltage is created with diode connected PMOS at 1st stage to weaken the pull-up strength of CPL.
  - Multi-threshold technology is used to further weaken the pull-up.

• **Limitations**
  - Speed degradation due to two stage operation
  - Use of multi-threshold technology is complex and expensive.

Ideation for CPLS

1) Key limitation of CPLS is the contention b/w pMOS & nMOS
2) How can we mitigate the contention?
3) Can we make the pull-up path significantly weaker?

\[ V_{DDH} \]
\[ V_{DDL} \]
\[ XL = 1.2V \]
\[ \text{IN} \]
\[ \text{INB} \]
\[ \text{OUT} = 0V \]
CPLS with Diode Connected PFET Insertion

• Goal
  • Diode MP3 and MP4 are added to limit the pull-up strength.
  • MN3 and MN4 guarantee full swing of OUTBH and OUTH nodes.

• Limitations
  • Static current path of MP2 and MN4 when IN=low.

Ideation for CPLS

1) Key limitation of CPLS is the contention b/w pMOS & nMOS
2) Can we make the pull-up path significantly weaker?
3) More effectively, only when $V_{DDL}$ is small!

$$V_{DDH} = V_{DDH}$$

$V_{DDL} = 0V$

$XL = 1.2V$

IN

INB

$V_{DDL}$

Pull-up CNTL

OUT
How Can We Control Pull-up Strength w/ $V_{DDL}$?

• Express your aim verbally!

👉 When $V_{DDL}$ is lower, pull-up should be weaker.

• Another conclusion: with nMOS + pull-up pMOS current mirror, we can control pull-up network with $V_{DDL}$. 
LS with Current Limiter

• **Goal**
  • Reducing the drive strength of pull-up network in CPLS by biasing $M_{P1}$ and $M_{P2}$ with intermediate voltage.

• **Limitations**
  • Static current in the bias voltage generation circuit.

Ideation for Current Limiter CPLS

1) Static current is wasted.

2) Can we make the pull-up controller is only turned on only when/where it is required?

Turning on MP1 and MP2 only when they are required.
How Can We Adaptively Control Pull-up Network?

- Focus on “where”

Turned on when IN is low
Turned off when IN is high

Turned on when INb is low
Turned off when INb is high
How Can We Block the Static Current?

- Still “when” should be addressed!
- After the transition finishes, MP1 and MP2 should be turned off back.

→ How can we detect whether the transition is finished?
Adaptive Current Limiter CPLS

• **Goal**
  - IN and OUT are compared to selectively supply the current to the path to be pulled up.

• **Limitations**
  - When IN=0, Q1 retains with float high, which makes vulnerable to noise.

1) Key limitation of CMLS is the static current when IN is high
2) Can we make block the short-circuit current after the transition finishes?

→ How can we detect whether the transition is finished?
Wilson’s Current Mirror Level Shifter

• Goal
  • Static current in CMLS is removed by feedback pMOS M5.

• Limitations
  • Rising time and rising level of output node (Z) is greatly degraded because V1 cannot be decreased sufficiently due to M5.
  • Out is float high when IN is high

Ideation for Improving Wilson’s CMLS

1) One problem is the rising performance of output node (Z) is greatly increased because V1 cannot be decreased sufficiently due to M5. 
   ➔ Can we delay the turn-off moment of M5 a little bit?

2) Another problem is OUT is floated high. ➔ Can we keep V1 low for high IN?
CMLS With Diode Chain

• Goal
  • Speed degradation and floating OUT problem in WCMLS are resolved

• Limitations
  • Trade-off between the static current vs. noise stability

Ideation for Improving Wilson’s CMLS

1) One problem is the rising performance of output node (Z) is greatly increased because V1 cannot be decreased sufficiently due to M5.

⇒ This means that OUT becomes only 0.9V... while it should be 1.2V.

⇒ Can we amplify the OUT?
CMLS + CPLS

• Goal
  • Speed degradation of OUT problem in WCMLS are resolved

• Limitations
  • The node A is still floated high.
  • Two stage operation limits the overall speed

Ideation for Improving Wilson’s CMLS

1) How about making V1 fall to full 0? Then we can achieve high speed OUT rising and OUT will not be floated.

2) By how?

![Circuit Diagram]

VDDH  VDDH
M6 M7
V1 OUT
M5
V2
M3 M4
IN INb

VDDH VDDH
X OUT
IN INb
Operation Verification For Rising

• When IN = 0 ➔ 1,
  1) OUT would be initially low, and X would be $V_{DDH} - |V_{thp}|$
  2) Although M2 is turned on, X can be easily pulled down, because M1 is initially off.
  3) Lowered X pulls up OUT, leading to turn off M2. Thus, X can be fully pulled-down to zero.
  4) OUT can be raised quickly and be driven full VDD without floating
Operation Verification For Falling

• When IN = 1 ➔ 0, (INb = 0➔ 1)
  1) OUT would be initially high, and X is initially 0V.
  2) Although OUT should be pulled down by rising INb, the contention prevents OUT from falling.
  3) Thus, level shifting may not occur (malfunction).

➡ How can we solve this?
Just Focus on the Problem! Ideation!

1) When \( IN = 1 \rightarrow 0 \), \((INb = 0 \rightarrow 1)\), \( OUT \) should be lowered.

2) Pull-up path can be blocked for the above case.

3) How can we implement it? \( \Rightarrow \) Express it verbally!

![Diagram](image)

Turns off when \( IN=0 \) & \( INb = 1 \)

Turns on when \( IN=1 \) & \( INb = 0 \)
How to Realize Through Circuit

1) We need ON & OFF; pMOS and nMOS both are required.
2) Can we directly connect IN? \(\Rightarrow\) **No! (Why?)**
3) How can we make the circuit controlled by \(V_{DDL}\) swing signal?
   \(\Rightarrow\) nMOS + pMOS current Mirror; but swing of the output is limited
   \(\Rightarrow\) We can utilize the restoring feature of the inverter!

![Circuit Diagram]

IN=0 : OFF \(\Rightarrow\) \(V_{DDH}\)
IN=1 : ON \(\Rightarrow\) 0V

How can we make this node full swing 0~\(V_{DDH}\)?
Static Current Free CMLS w/ LECC

- Logic error detection circuit is employed to control M4

Summary

• Level shifter is required to stably transfer the signal across different VDD domain.

• The conventional level shifters have two main limitations; CPLS has limited voltage range while CMLS consumes large static power.

• In order to resolve the limitations of the conventional LSs, there are many level shifters proposed.

• We saw the step by step ideation procedure for each level shifter development.