Power (3)

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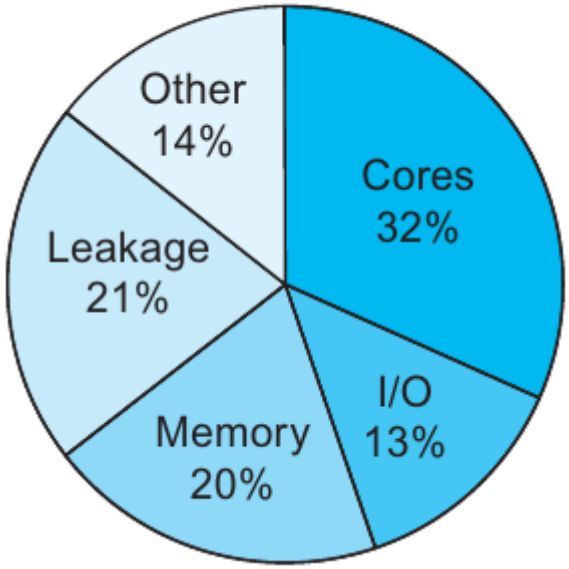


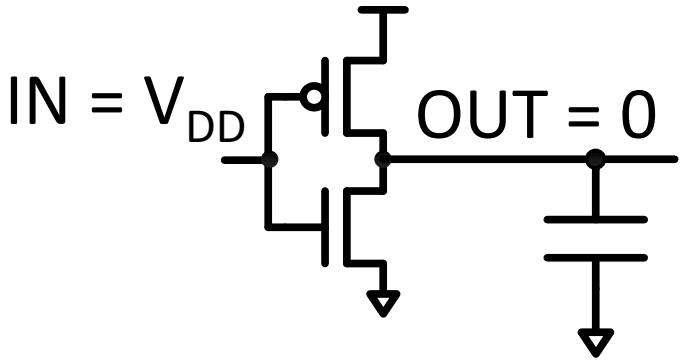
Static Power

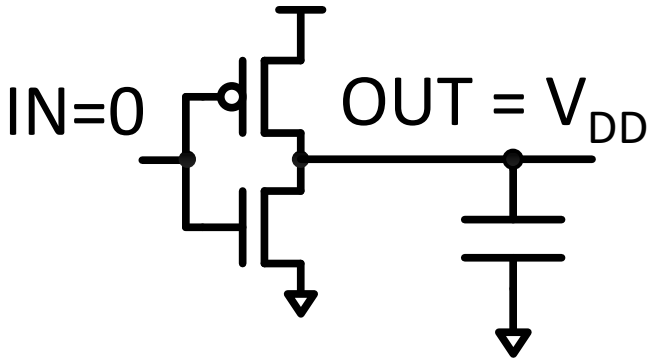
- ✓ Power still consumed when circuit does not operate. Why?
- ✓ Leakage current paths in MOSFETs
- ✓ Solutions for reducing static power

Power is Kept Consumed. Why?

- Suppose that IN is kept high or low in CMOS inverter.
- Then, pMOS or nMOS are respectively turned off. But there is still current flowing. Why?

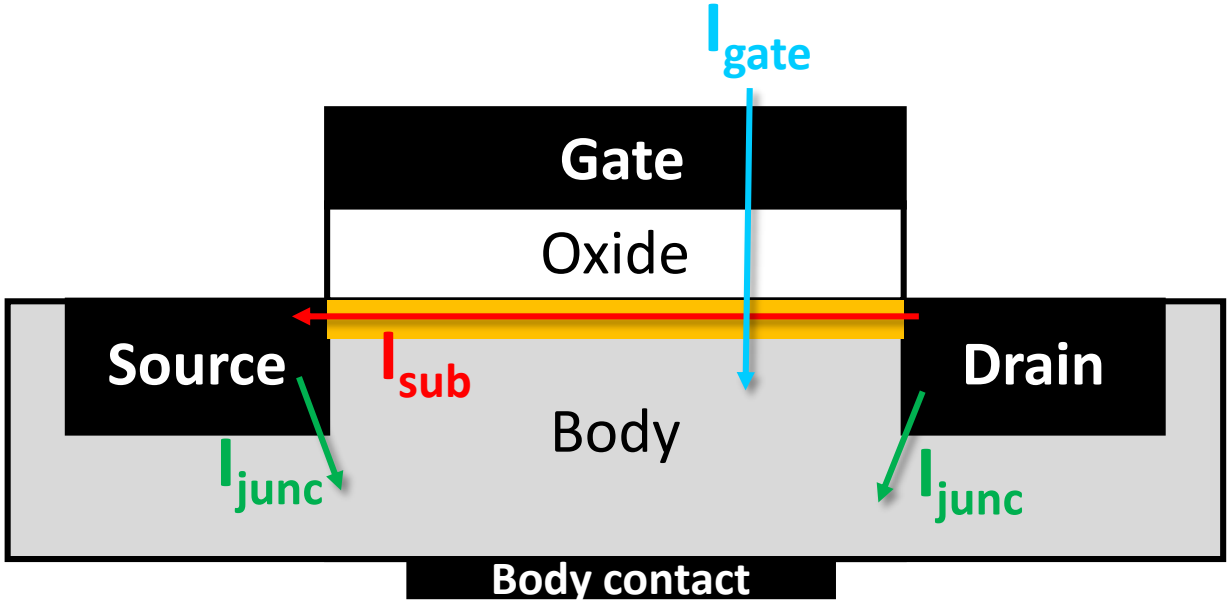
➔ MOSFET is not ideal, thus **leakage current** flows.





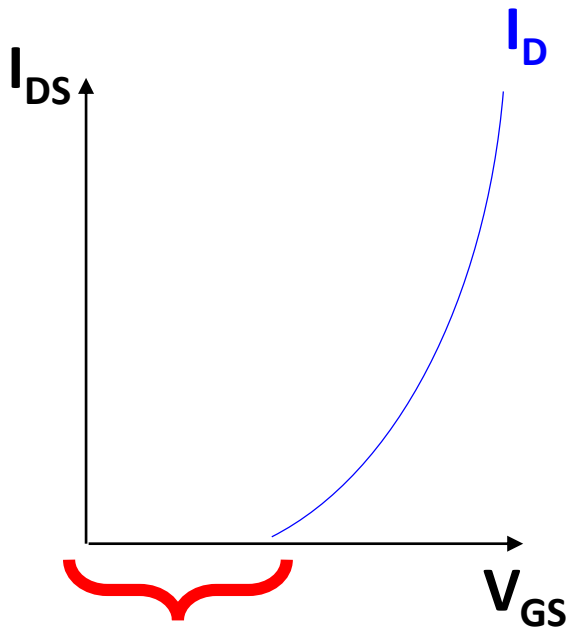
Leakage Current Paths

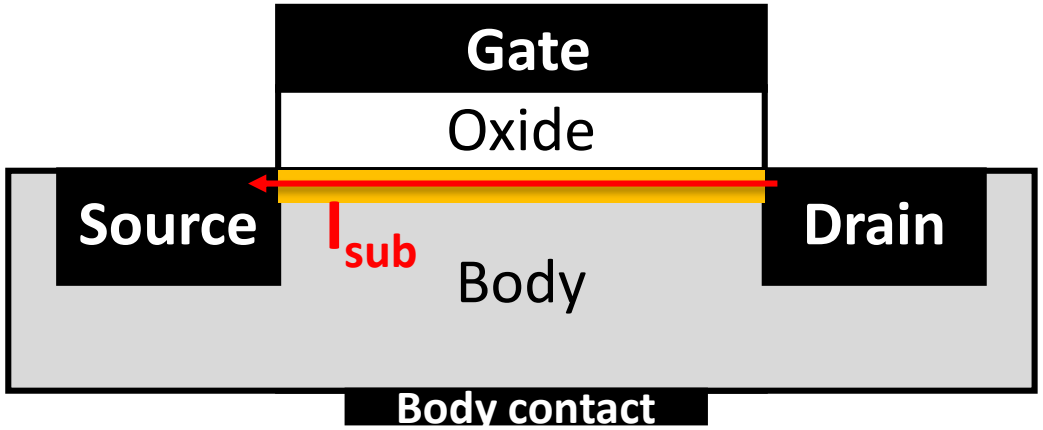
- **Sub-threshold current** I_{sub} = Drain to Source current even when $V_{GS} < V_{th}$
- **Gate leakage** I_{gate} = Gate to body current
- **Junction leakage** I_{junct} = Drain/Source to body current



Sub-threshold Leakage

- In real transistors, current does not abruptly cut off below threshold, but rather drops off exponentially.

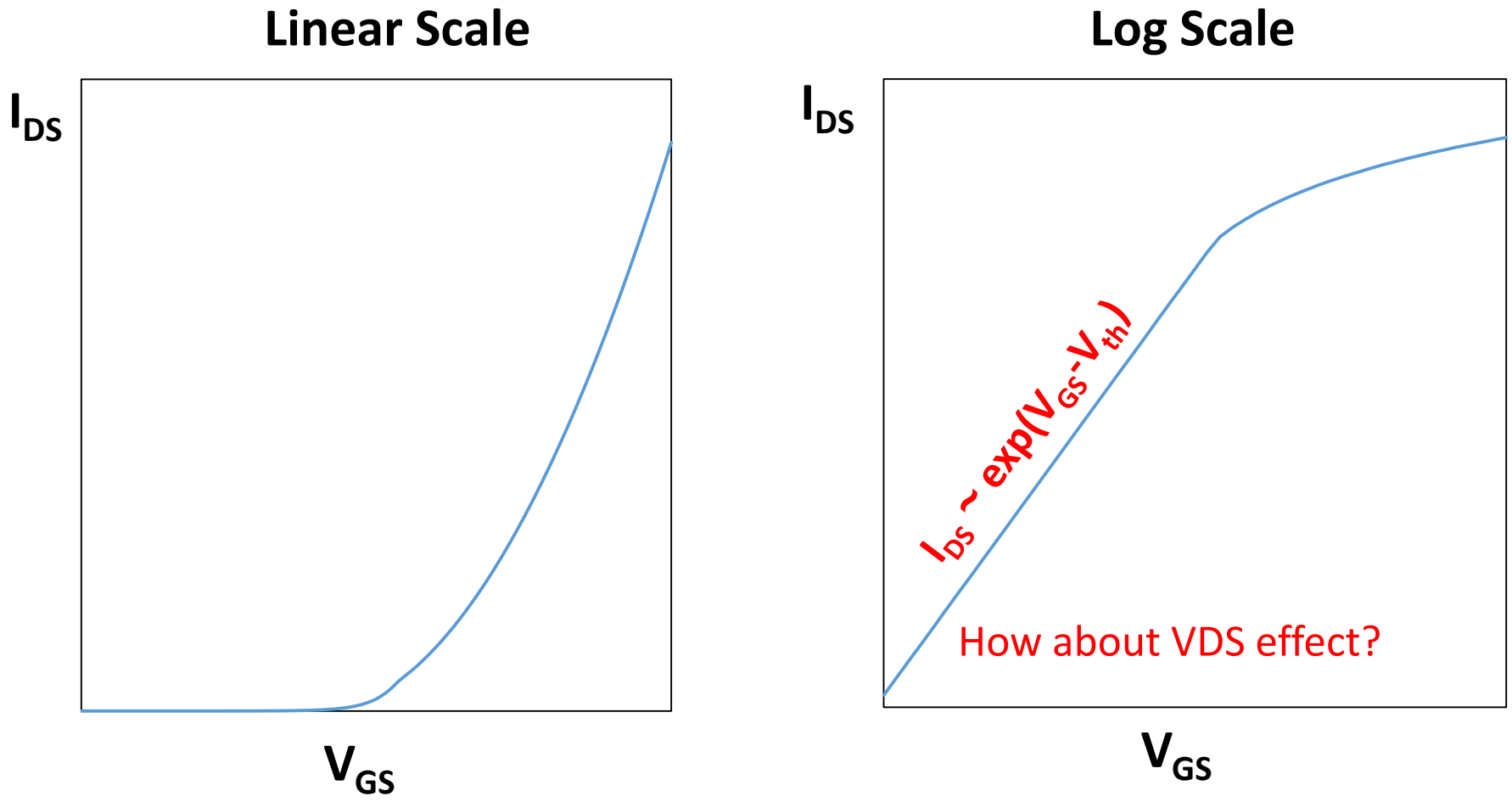




How about here? $V_{GS} < V_{th}$

$I_D = 0$?

Exponential Dependence of I_{DS} on V_{GS}



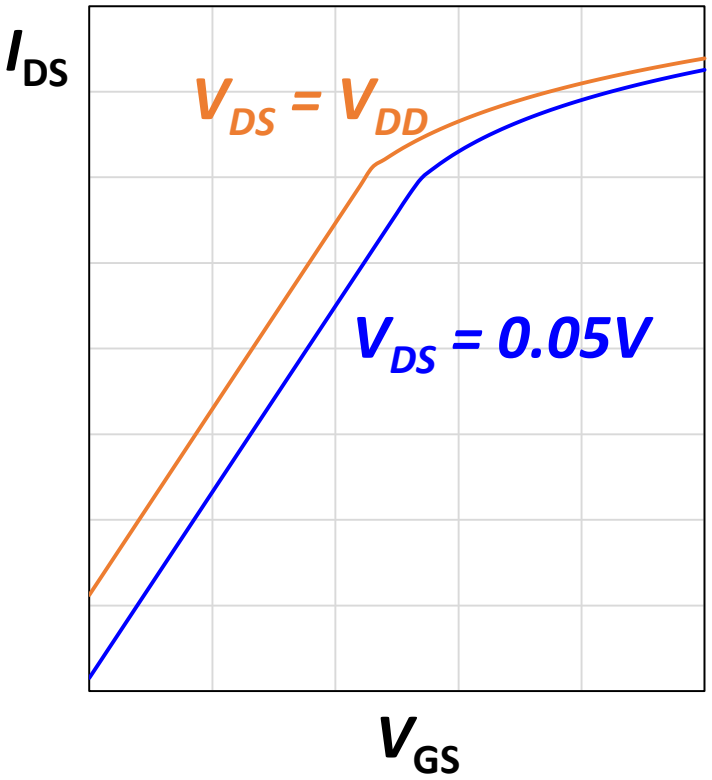
Subthreshold I_{DS} vs. V_{DS}

- There is a drain-induced barrier lowering (DIBL).
  ➔ Current flow exceedingly increases by large V_{DS}.
- We can define V_{th} to be dependent on V_{DS} to consider DIBL

$$V_{th} = V_{th0} - \eta V_{DS}$$

- Then, I_{sub} is represented as

$$I_{Sub} = I_{DS0}\exp\left(\frac{V_{GS}-V_{th}}{nV_T}\right)\left\{1-\exp\left(\frac{-V_{DS}}{V_T}\right)\right\}$$



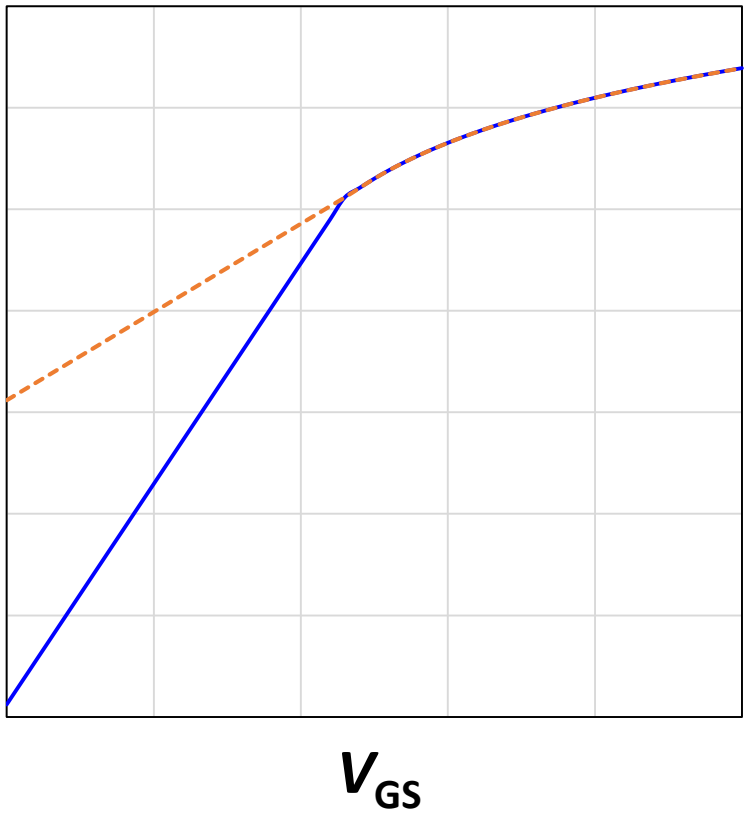
Subthreshold Swing;
Characterize Sub-Threshold Region Feature

- Which is better?
- We can represent this goodness of subthreshold feature using a parameter sub-threshold swing (SS).
- SS indicates how much V_G must drop to decrease I_{sub} by 1/10x.

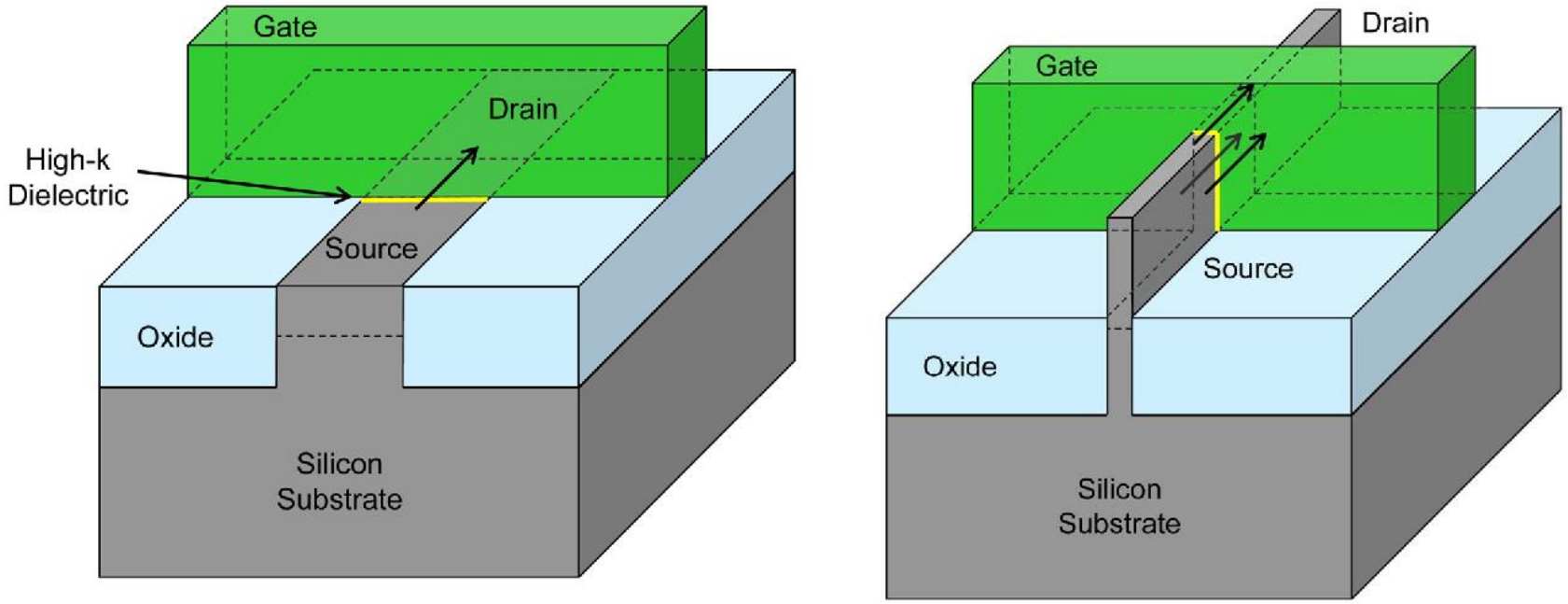
$$SS = \left[\frac{d\left(\log_{10} I_{ds}\right)}{dV_{gs}} \right]^{-1} = nv_T \ln 10$$

- I_{Sub} can be expressed using SS as

$$I_{Sub} = I_{DS0} 10^{\left(\frac{V_{GS}-V_{th}}{SS}\right)} \left\{ 1\text{-}\exp\left(\frac{-V_{DS}}{V_T}\right) \right\}$$



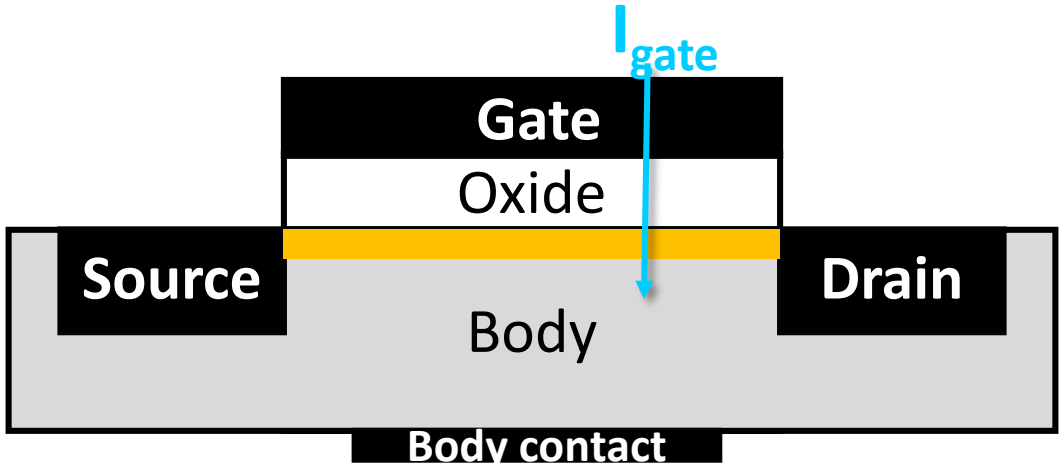
Revisit FinFET vs. planar MOSFET



Gate Leakage

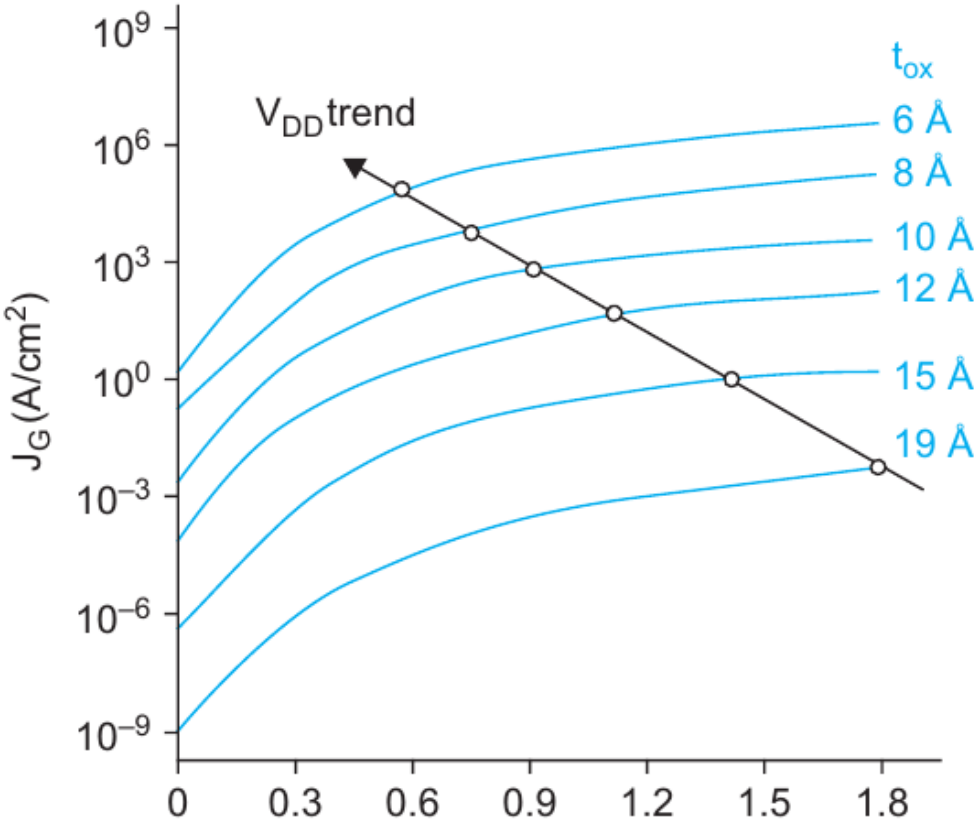
- Due to tunneling, when V_{GC} is large, leakage flows through oxide.
- Can you expect the effect of W, V_{GC} or t_{ox} on I_{gate}?
- When $V_{GC} = V_{DD}$, I_{gate} by tunneling is estimated as

$$I_{\text{gate}} = WA\left(\frac{V_{DD}}{t_{\text{ox}}}\right)^2 \text{e}^{-B\frac{t_{\text{ox}}}{V_{DD}}}$$



Gate Leakage Trend

- Why does t_{ox} decrease?



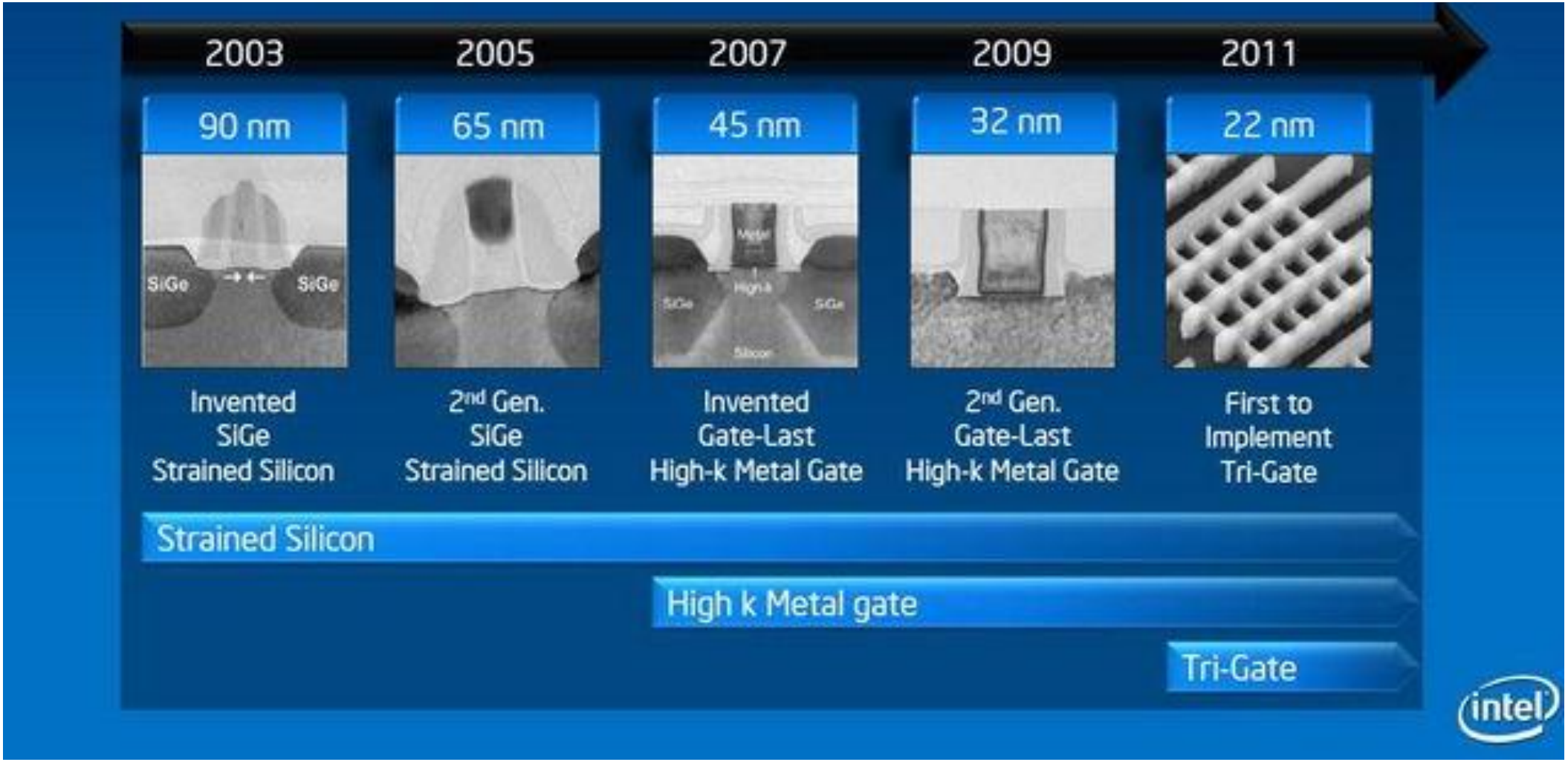
Motivation for Using High-K Dielectric

- Is there any way to reduce I_{gate} while increase I_{on}?

$$I_{\text{gate}} = WA\left(\frac{V_{DD}}{t_{\text{ox}}}\right)^2 e^{-B\frac{t_{\text{ox}}}{V_{DD}}} \quad \textbf{vs.} \quad I_{on} = \frac{1}{2}\mu\left(\frac{\varepsilon_{ox}}{t_{ox}}\right)\left(\frac{W}{L}\right)(V_{GS}-V_{th})^2$$

Material	Permittivity	Material	Permittivity
Si_3N_4	7[5,8]	La_2O_3	20-30[5,8]
Al_2O_3	9[5,8]	PrO_x	30[23]
ZrO_2	14-25[8]	Gd_2O_3	9-14[8]
HfO_2	15-26[8]	Other Ln_2O_3 (Ln=Nd, Sm, Dy, Ho, Er, Yb, Lu)	9-14[8,24]
Y_2O_3	12-15[5,8]	$REScO_3$	20-22[21]

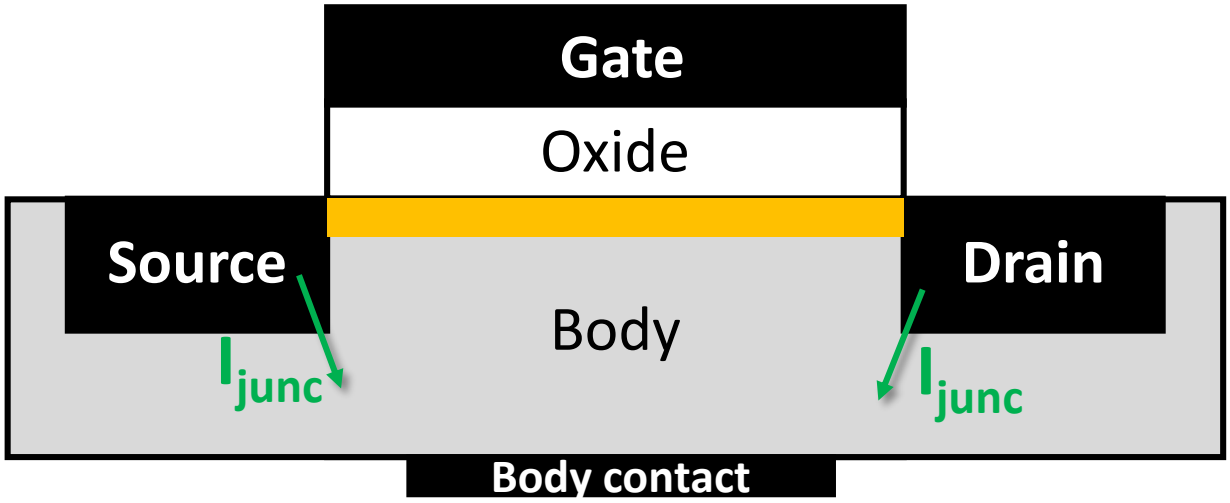
MOSFET Innovation by Intel



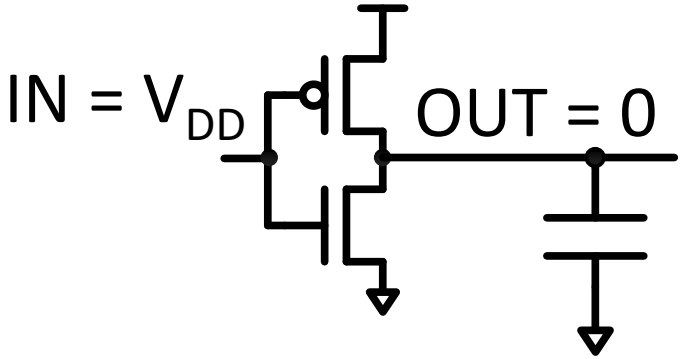
Junction Leakage

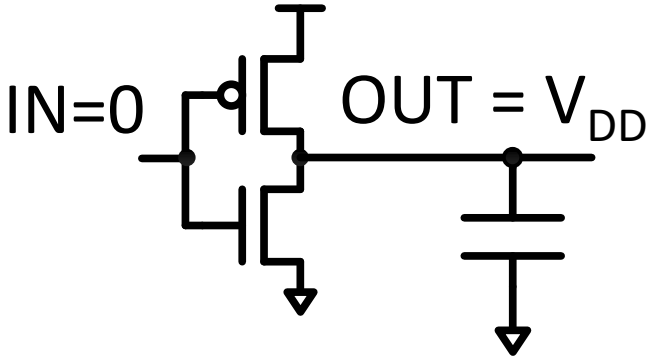
- Even in the reverse bias, ID flows due to band-to-band tunneling and gate-induced drain leakage (GIDL)

$$I_D = I_S\left(e^{\frac{V_D}{v_T}} - 1\right)$$



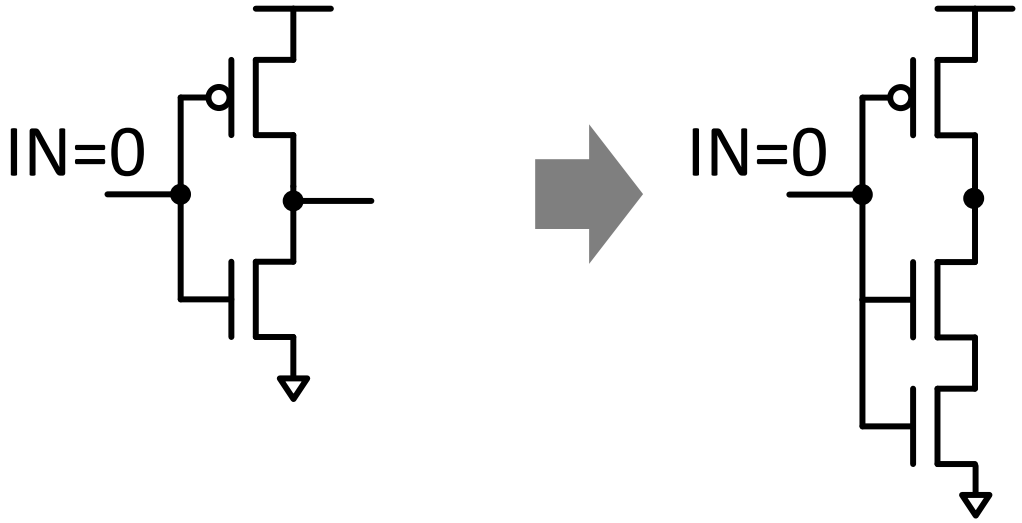
Now, Revisit This!





Reducing Isub by Stack Effect

- How will the I_{sub} change if we use stacked MOSFETs for an inverter?



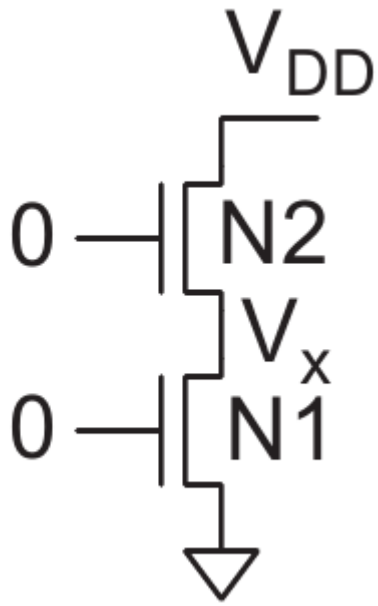
I_{sub} Reduction with Stack Effect

- I_{off} is I_{sub} when $V_{GS} = 0$ and $V_{DS} = V_{DD}$ for single MOSFET.

$$I_{sub} = \underbrace{I_{off} 10^{\frac{\eta(V_x - V_{DD})}{S}}}_{N2} = \underbrace{I_{off} 10^{\frac{-V_x + \eta\left((V_{DD} - V_x) - V_{DD}\right) - k_\gamma V_x}{S}}}_{N1}$$

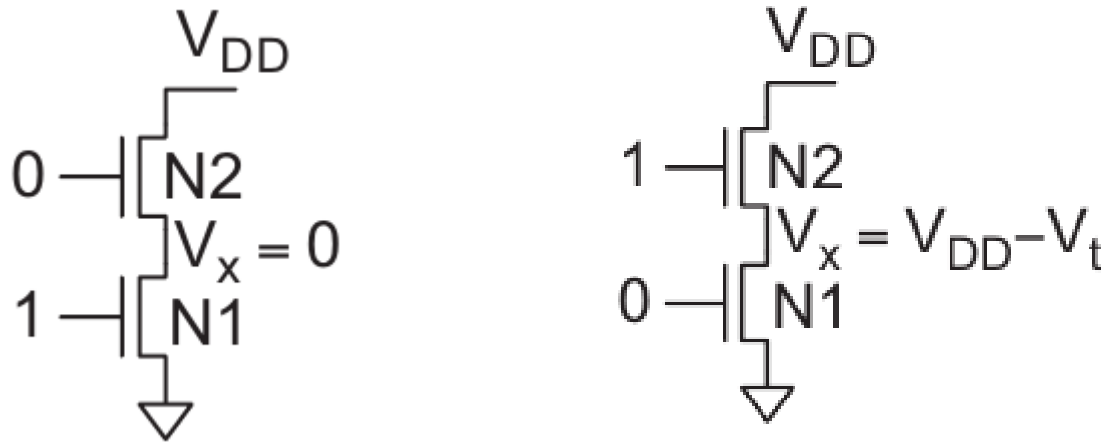
$$V_x = \frac{\eta V_{DD}}{1 + 2\eta + k_\gamma}$$

$$I_{sub} = I_{off} 10^{\frac{-\eta V_{DD}\left(\frac{1+\eta+k_\gamma}{1+2\eta+k_\gamma}\right)}{S}} \approx I_{off} 10^{\frac{-\eta V_{DD}}{S}}$$



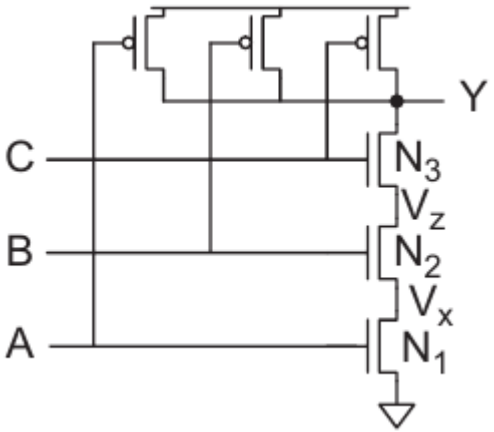
Gate Leakage in MOSFET Stack

- Which case does suffer larger gate leakage?



I_{gate} and I_{sub} in NAND3

- I_{gate} in nMOS = 6.3nA
- I_{sub} in nMOS transistor with $V_{DS} = V_{DD}$ = 5.63 nA
- I_{sub} in pMOS transistor with $|V_{DS}| = V_{DD}$ is 9.3 nA

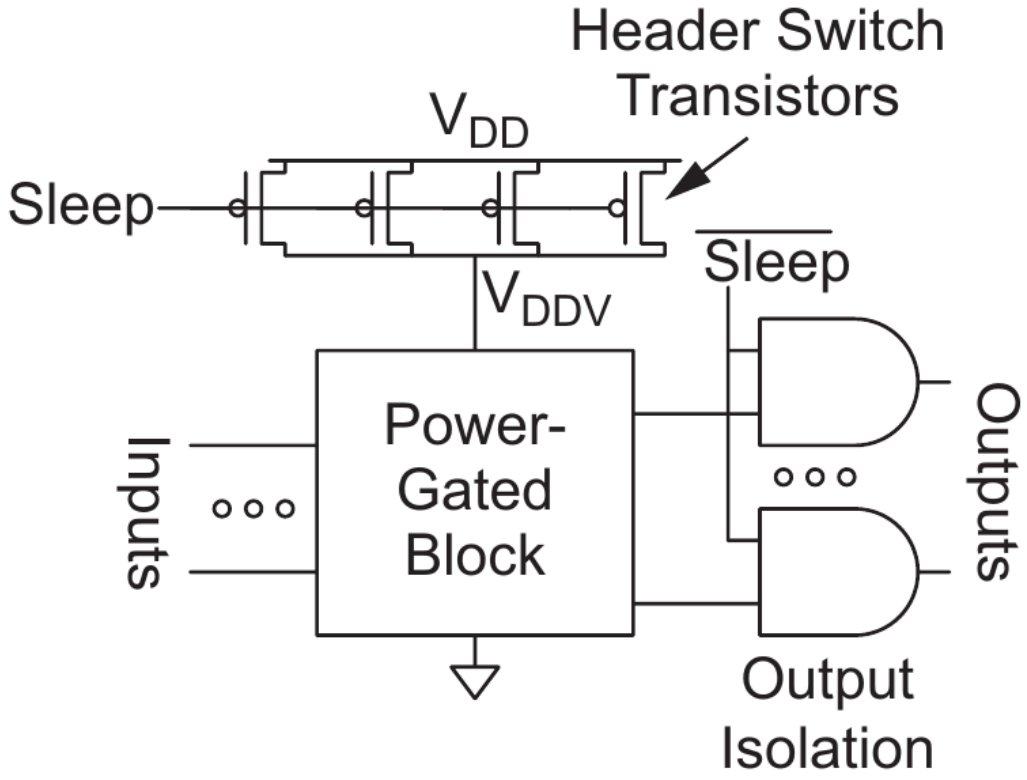


(nA)

Input State (ABC)	I_{sub}	I_{gate}	I_{total}	V_x	V_z
000	0.4	0	0.4	stack effect	stack effect
001	0.7	0	0.7	stack effect	$V_{DD} - V_t$
010	0	1.3	1.3	intermediate	intermediate
011	3.8	0	10.1	$V_{DD} - V_t$	$V_{DD} - V_t$
100	0.7	6.3	7.0	0	stack effect
101	3.8	6.3	10.1	0	$V_{DD} - V_t$
110	5.6	12.6	18.2	0	0
111	28	18.9	46.9	0	0

Power Gating

- The switch has an effective resistance that inevitably causes some voltage droop on V_{DDV} and increases the delay
- The switch is commonly sized to keep this delay to 5–10%.



Example 5.5

A cache in a 65 nm process consumes an average power of 2 W. Estimate how wide should the pMOS header switch be if delay should not increase by more than 6%?

- Assume that
  - pMOS on resistance is 2kΩ·µm
  - V_{DD} = 1V, and $|V_{th}|$ = 0.3V

Multiple Threshold Voltage & Oxide Thickness

- Generally, multiple threshold voltage devices are provided for circuit design.
  ➔Using multiple thresholds requires additional implant masks that add to the cost of a CMOS process.
- Most nanometer processes offer a thin oxide for logic transistors and a much thicker oxide for I/O transistors that can withstand higher voltages.
- The oxide thickness is controlled by another mask step. Gate leakage is negligible in the thick oxide devices, but their performance is inadequate for high speed logic applications. Some processes offer another intermediate oxide thickness to reduce gate leakage.