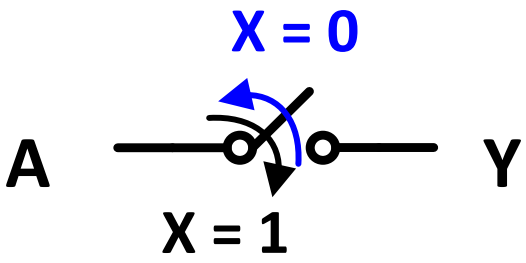
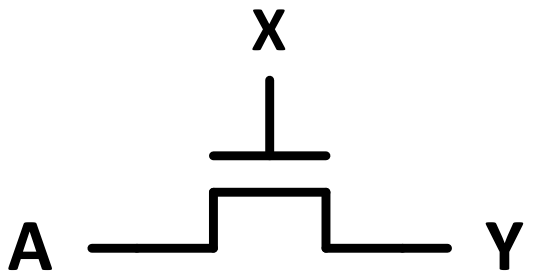
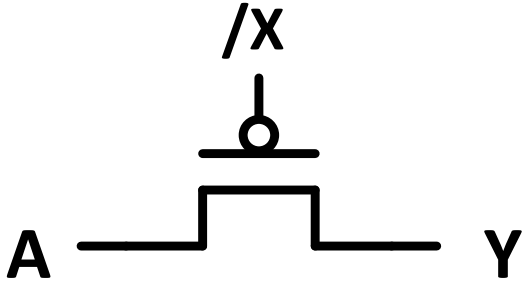
Switch

- How is it implemented?

➔ Of course, Transistor! nMOSFET or pMOSFET?



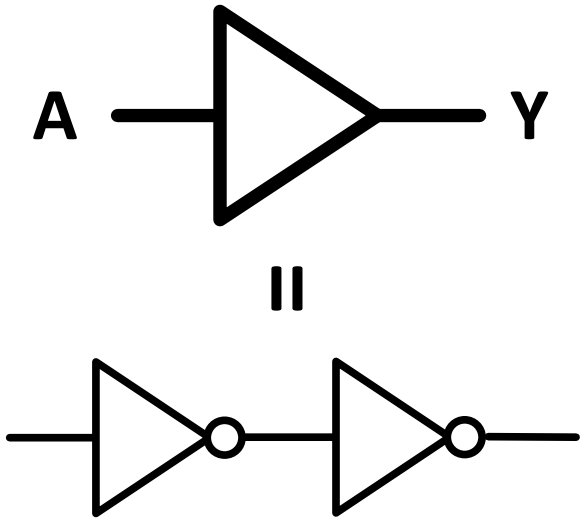




Buffer

- Have you seen the gate looking like below? Why is it useful?
- Can't we just use a switch?

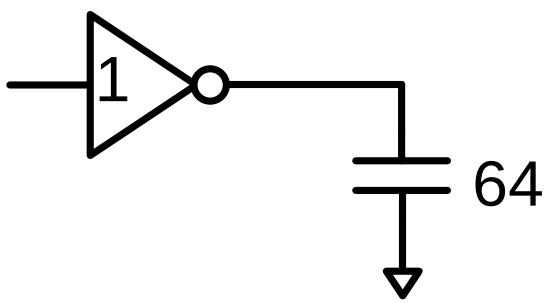
➔ You may be able to tell why. Do you remember that larger stage of N does not necessarily increase delay?

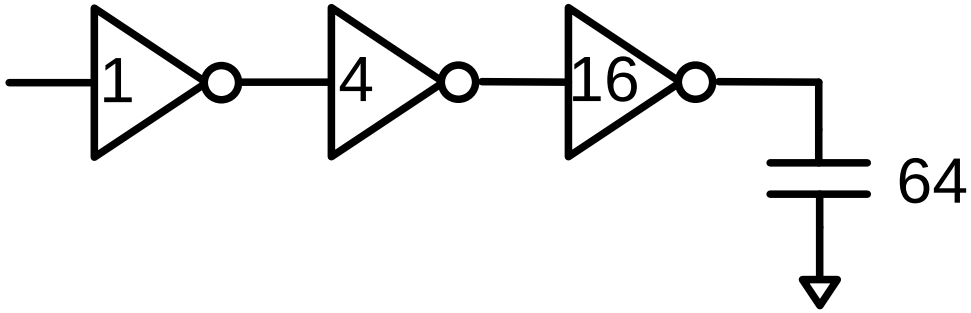


A	Y
0	0
1	1

Which is Faster?

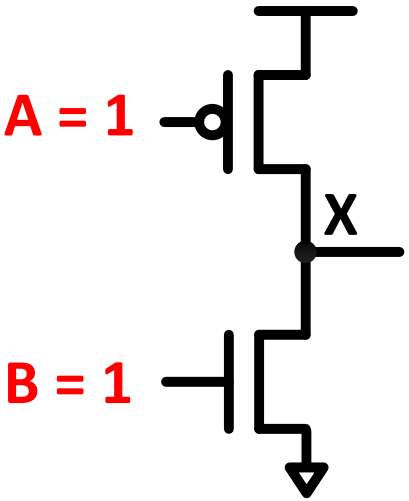
- The below example explains why we use a buffer.

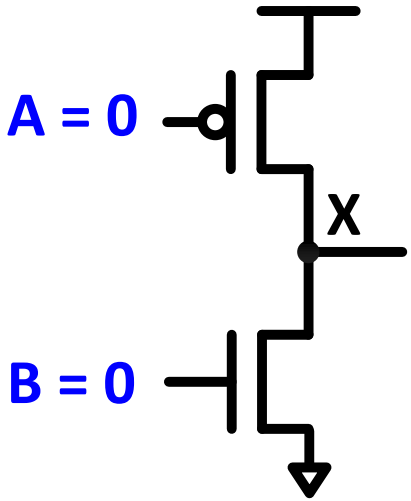


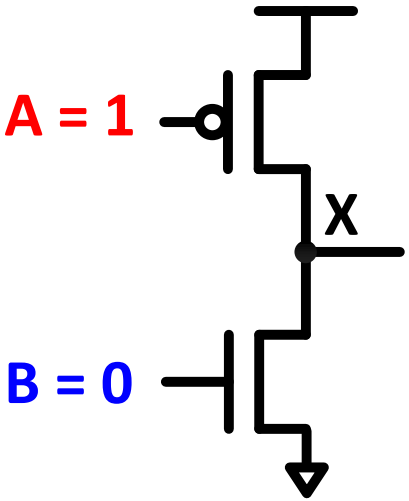


Floating & Contention

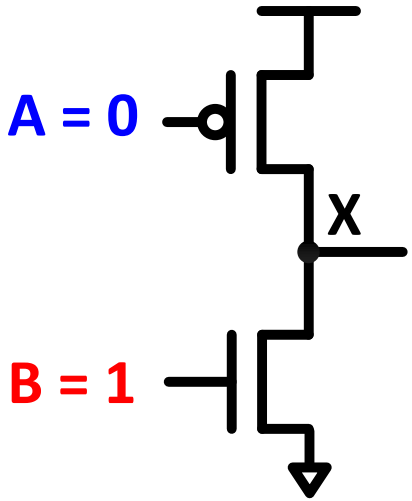
- What would be the voltage of X in the following situation?







Floating



Contention

Switch, Buffer, & Tri-states

Hanwool Jeong

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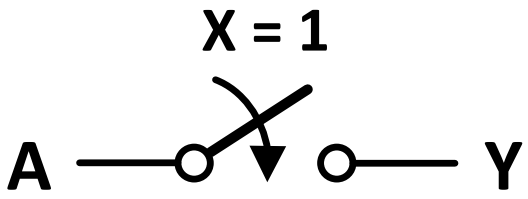
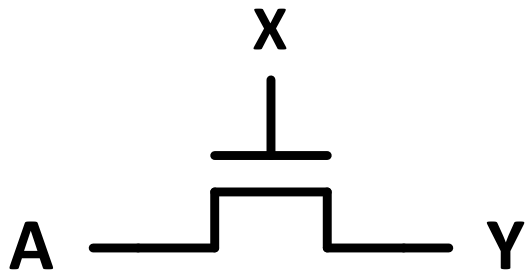
Switch Implementation

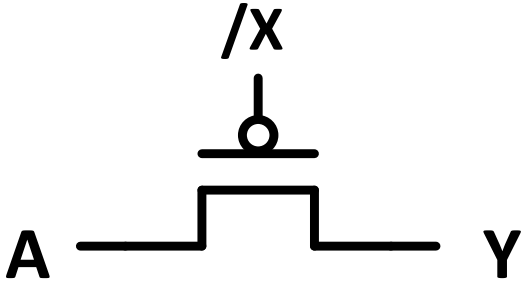
- ✓ Pass transistor; single nMOSFET or pMOSFET based switch
- ✓ Issues in pass transistor
- ✓ Transmission gate; switch without problem of pass transistor

Potential of MOSFETS as a Switch Operation





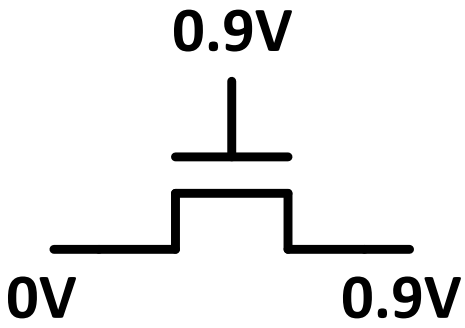
Turn on if $V_{GS} > V_{thn}$
Turn off if $V_{GS} < V_{thn}$



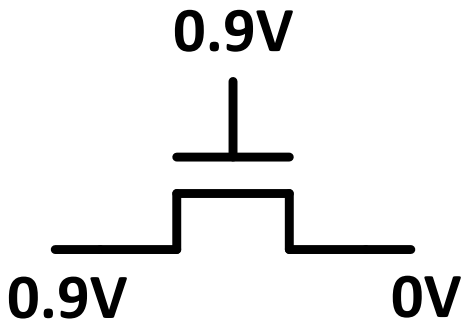
Turn on if $V_{SG} < |V_{thp}|$
Turn off if $V_{SG} > |V_{thp}|$

$V_{GS} \leqq V_{th}$ in nMOSFET

- Note that the structure of MOSFET is symmetric.



Is this TR turned on?
How does the current flow?

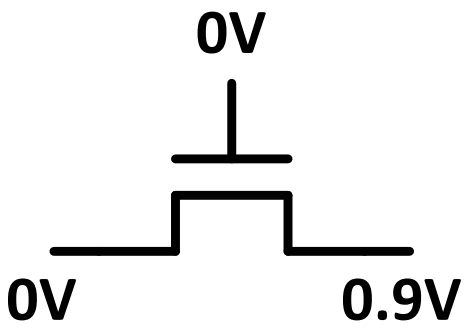


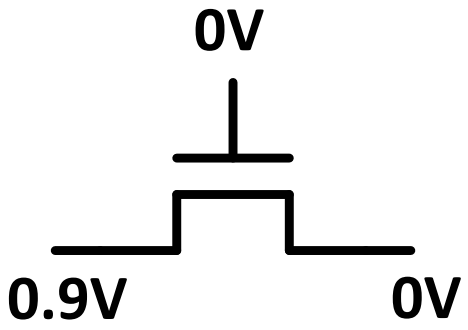
How about this?

- Can you reconsider the concept of source/drain?

$V_{GS} \lesseqgtr V_{th}$ in pMOSFET

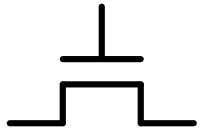
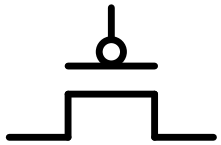
- Repeat that in the pMOSFET case!





We Can Just See The Gate Level

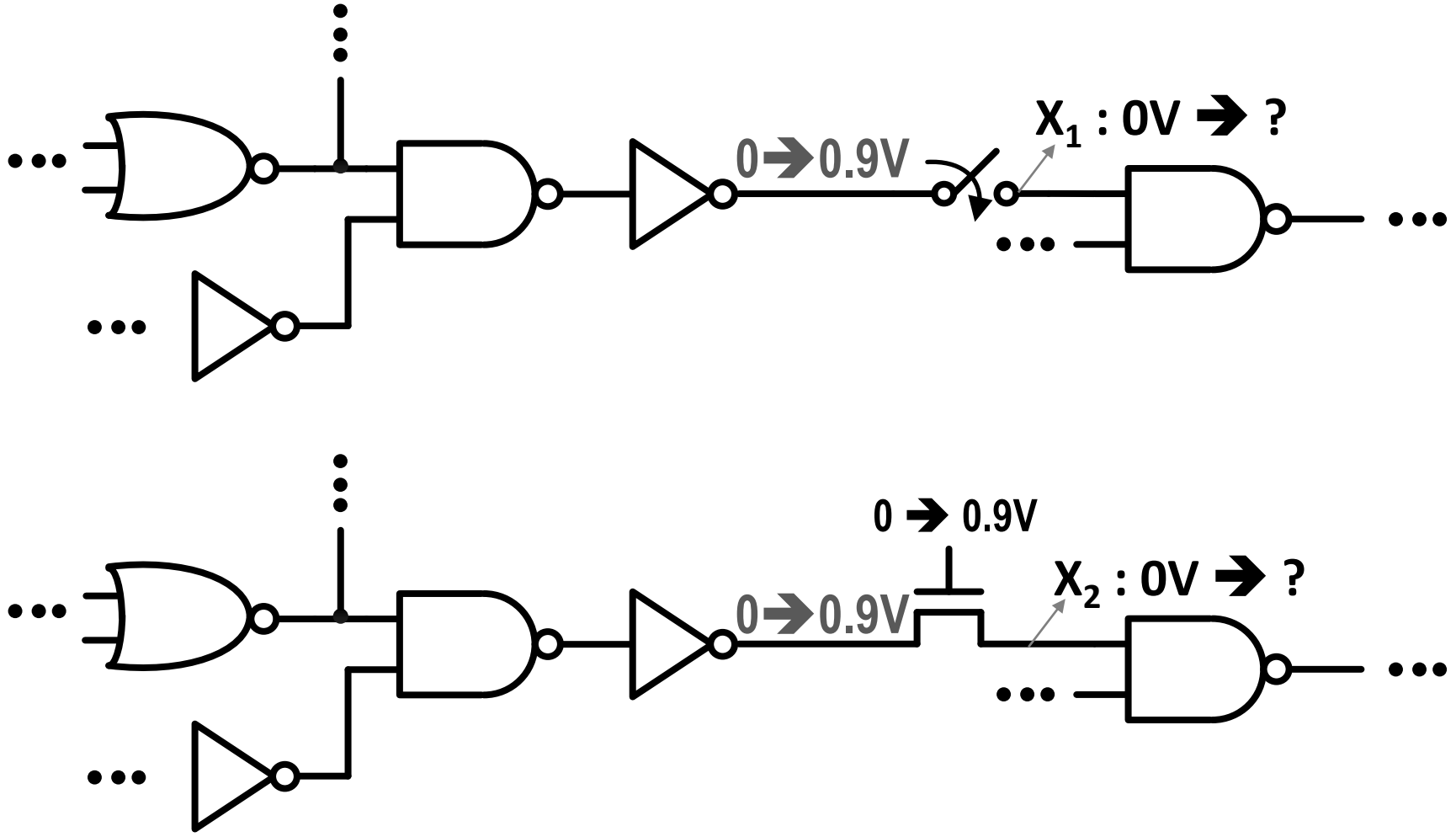
- No need to care about which are source or drain sides.
- You remember the following?

	$V_G = V_{DD}$	$V_G = 0$
		
		

- **More important thing is why the above table is not accurate.**

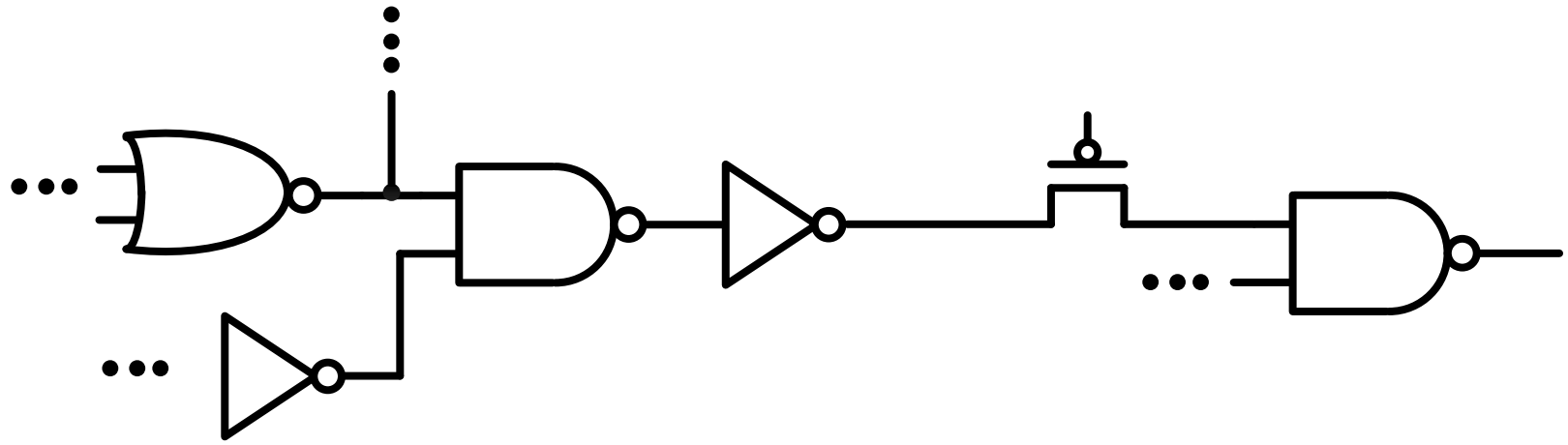
When You Realize Switch Through an nMOSFET or pMOSFET

- When V_{DD} = 0.9V, “0” and “1” represent 0V and 0.9V, respectively.



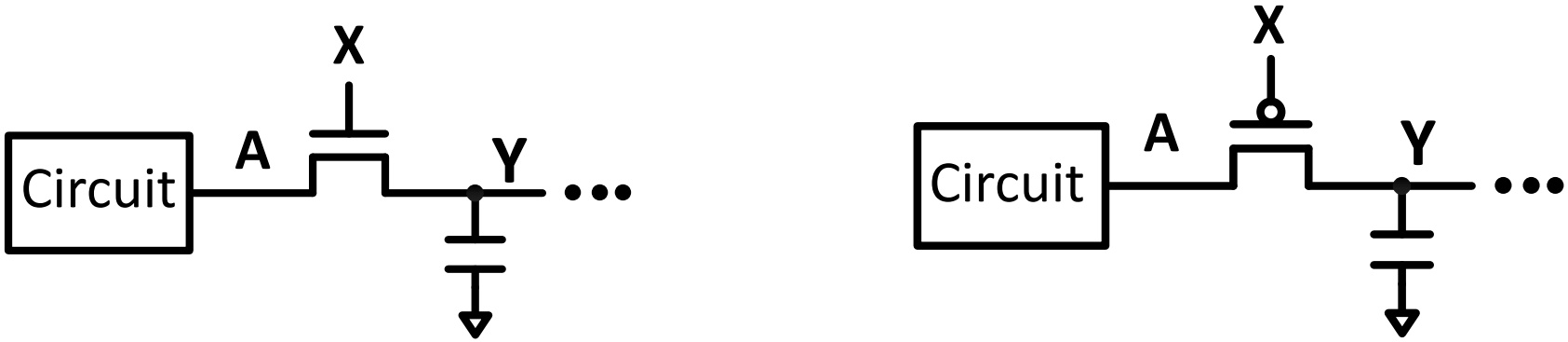
Then, Let's Replace it with pMOSFET

- Is it okay?



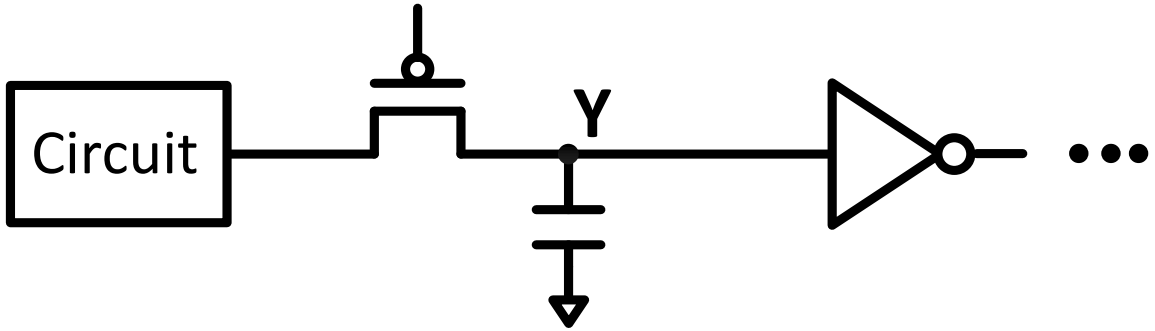
Vth Drop Across Transistor

- You can summarize the problem as
  - pMOSFET switch can deliver “1” well but “0” very poorly.
  - nMOSFET switch can deliver “0” well but “1” very poorly.



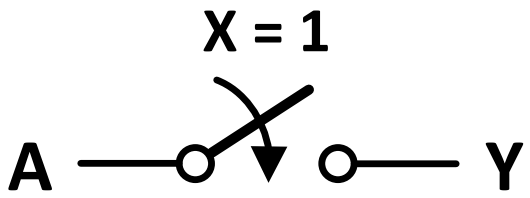
Why is it Problematic?

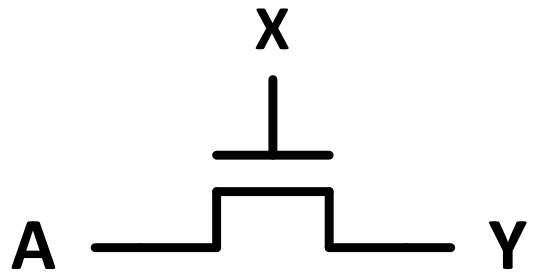
- Suppose that what happens if it is connected to another gate as an input.

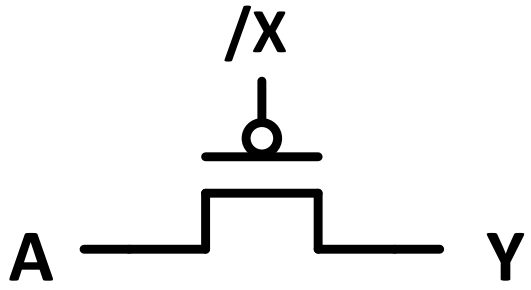


Pass Transistor

- They are widely used anyway. However, you must consider their limitations.





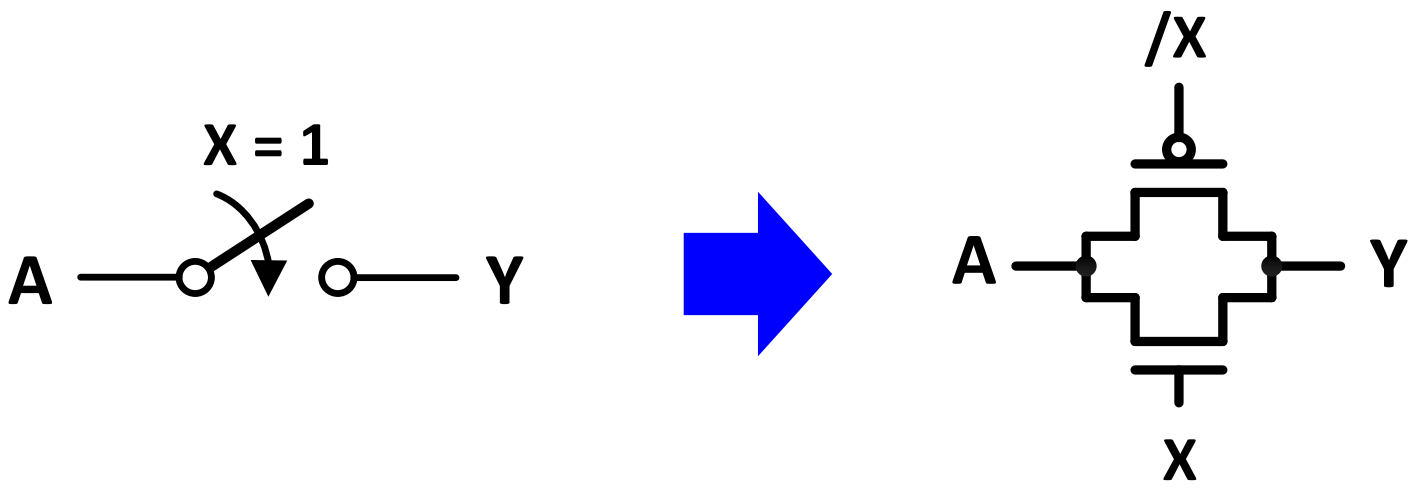


➔ **Is there any way we can deliver both “0” and “1” well?**

Diode Connected MOSFET

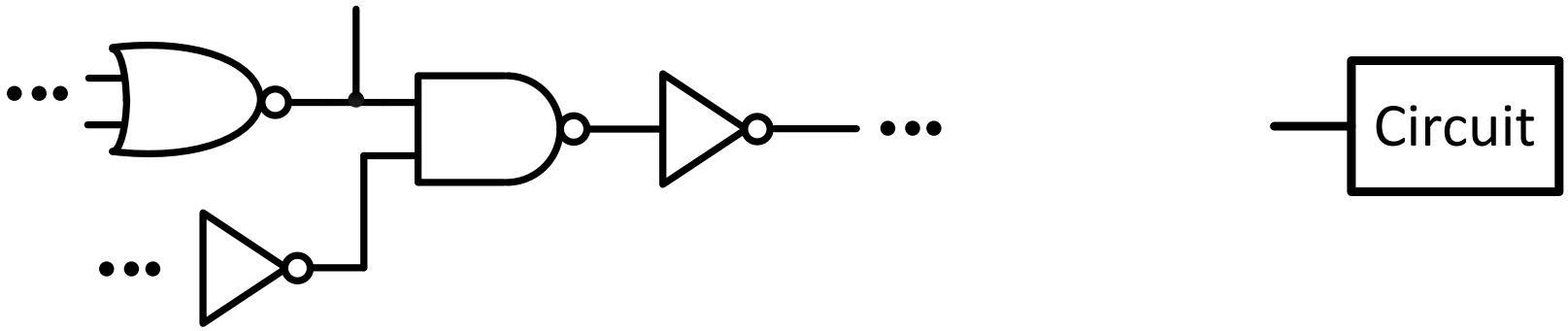
Transmission Gate

- Either for “1” or “0,” signal can be transferred without loss.

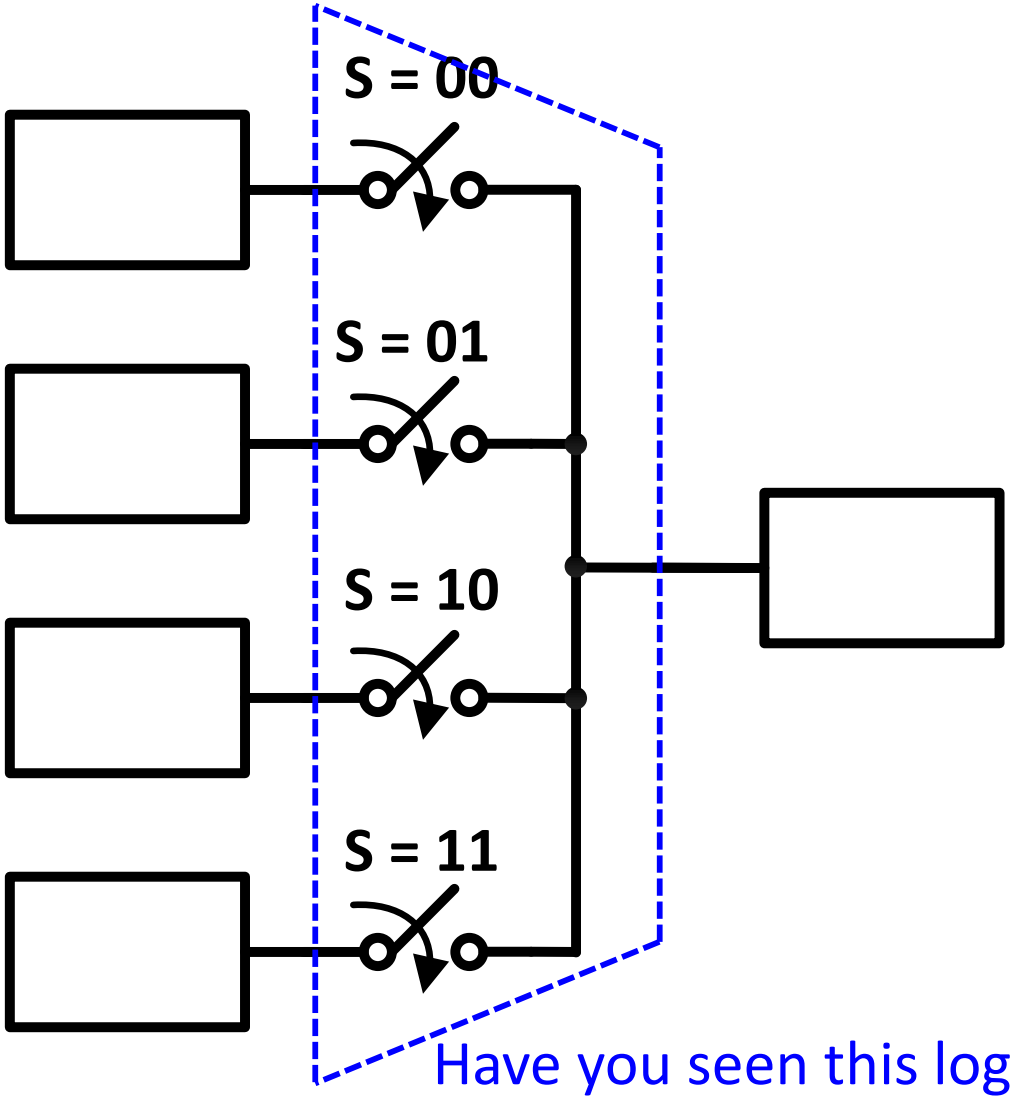


When Do We Need Pass TR or Transmission Gate?

- Certain path should be connected only for specific conditions.
- **Otherwise, it should "disconnect" the path (More important).**



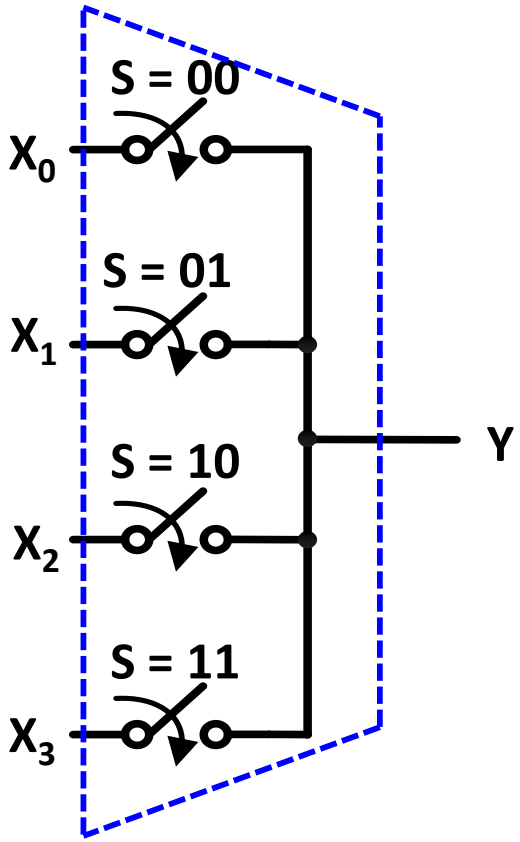
Selective Connection

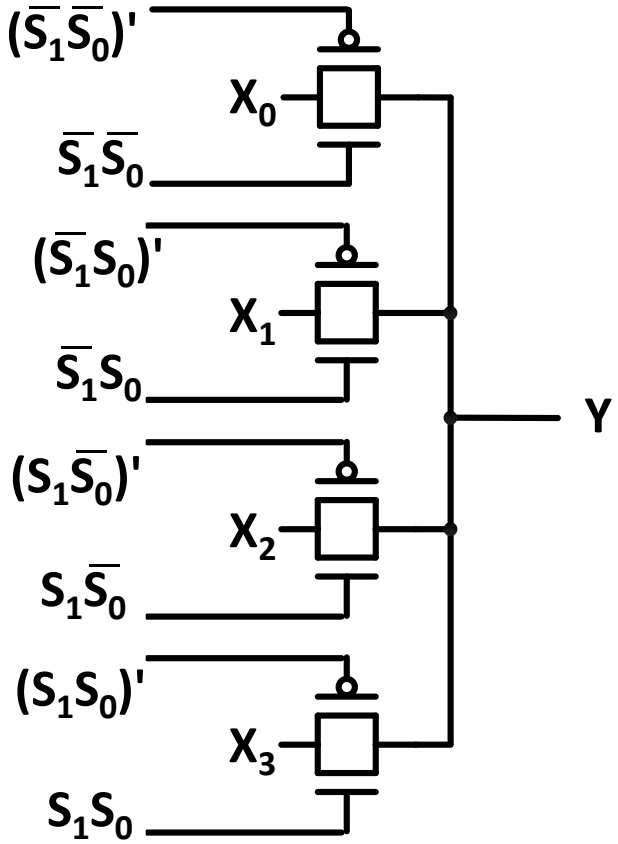


Have you seen this logic before?

Multiplexer (MUX)

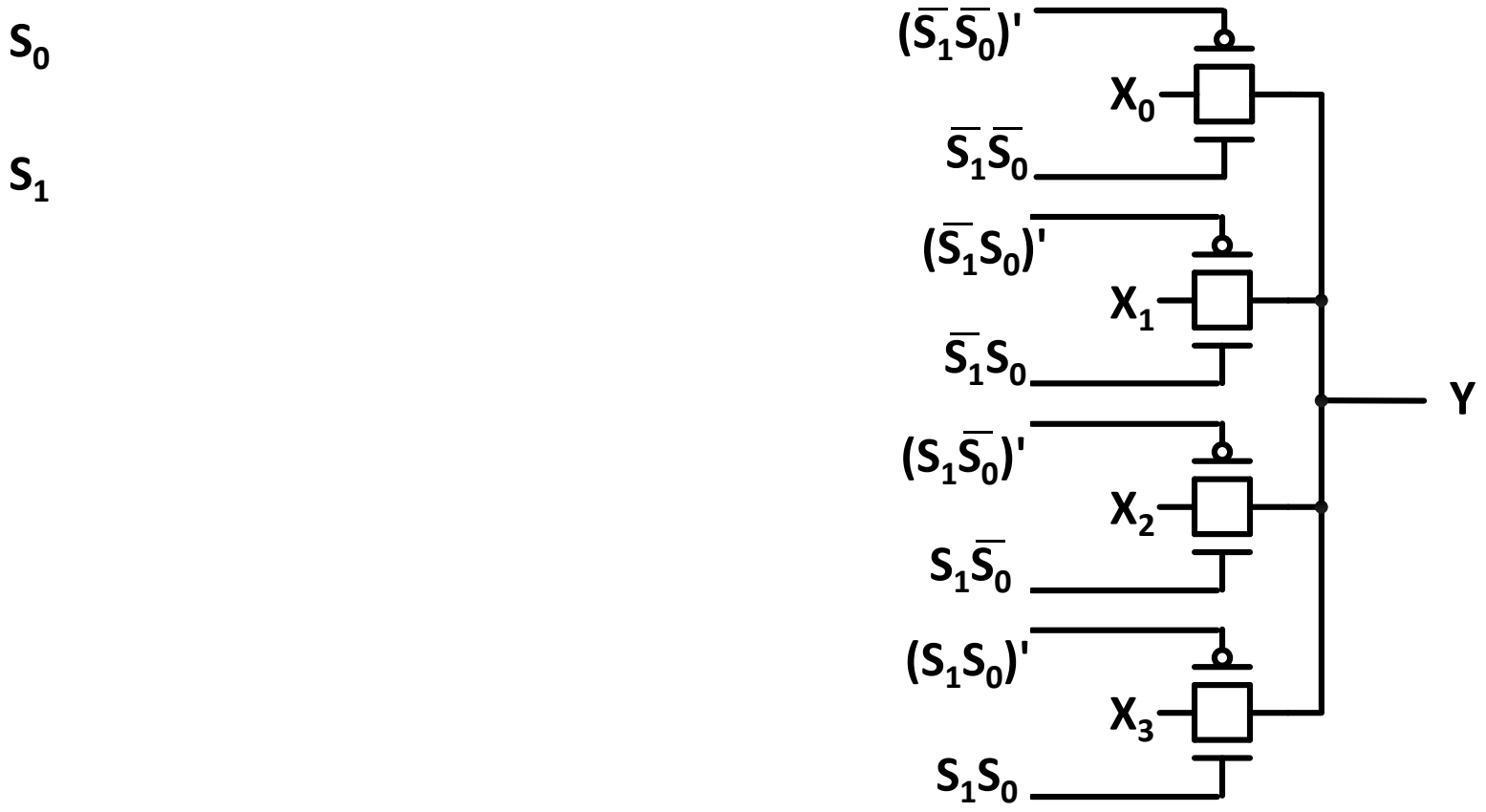
- **MUX** chooses the output from among inputs based on a select signal.





Selection Signal Circuit

- Given 2bit S input – S_1, S_0 – how can we implement a 4:1 MUX?



Speed and Signal Integrity of Transmission Gate

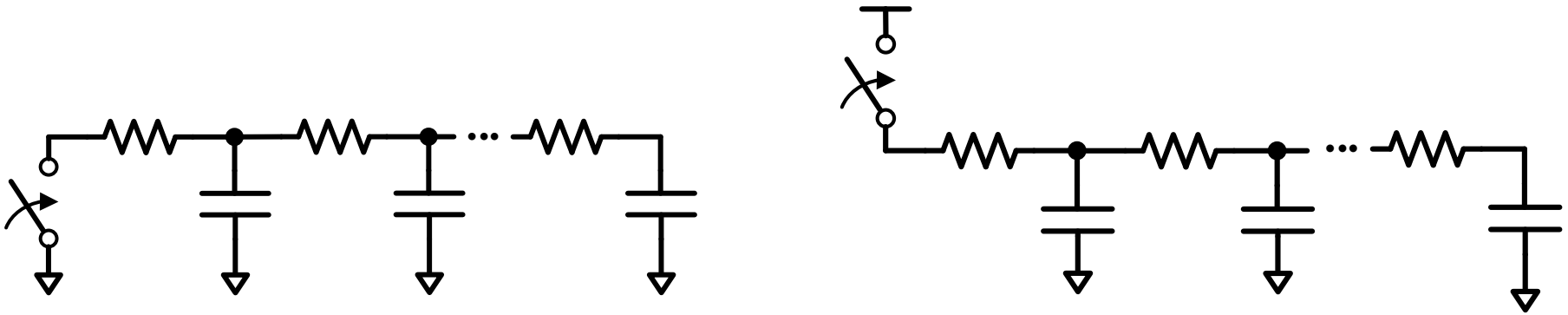
- ✓ Speed issue of transmission gate compared to CMOS inverter
- ✓ Signal integrity issue of transmission gate compared to CMOS inverter

Design Considerations

- Using Transmission gate may degrade the speed (Not always), and signal slope
- Using Transmission gate increases the noise sensitivity.

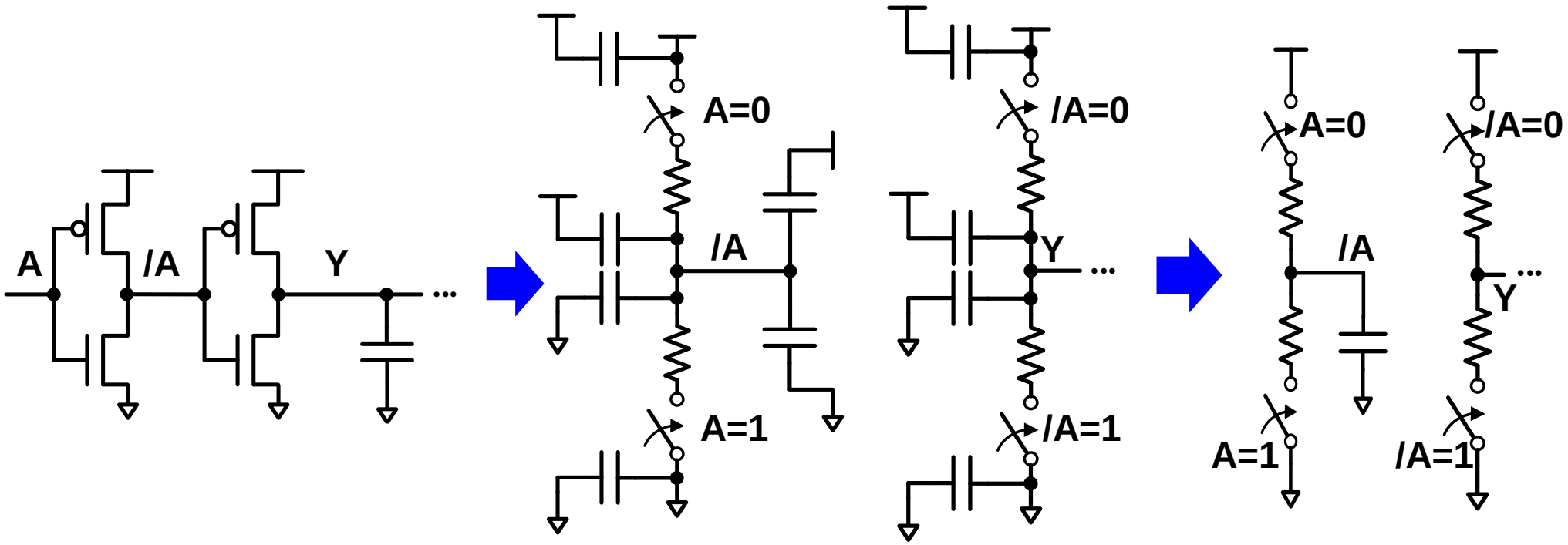
Revisit the RC Tree

- Elmore delay is determined as $\Sigma R_i C_i$
- Or simply, an increase in R or C degrades the signal propagation.



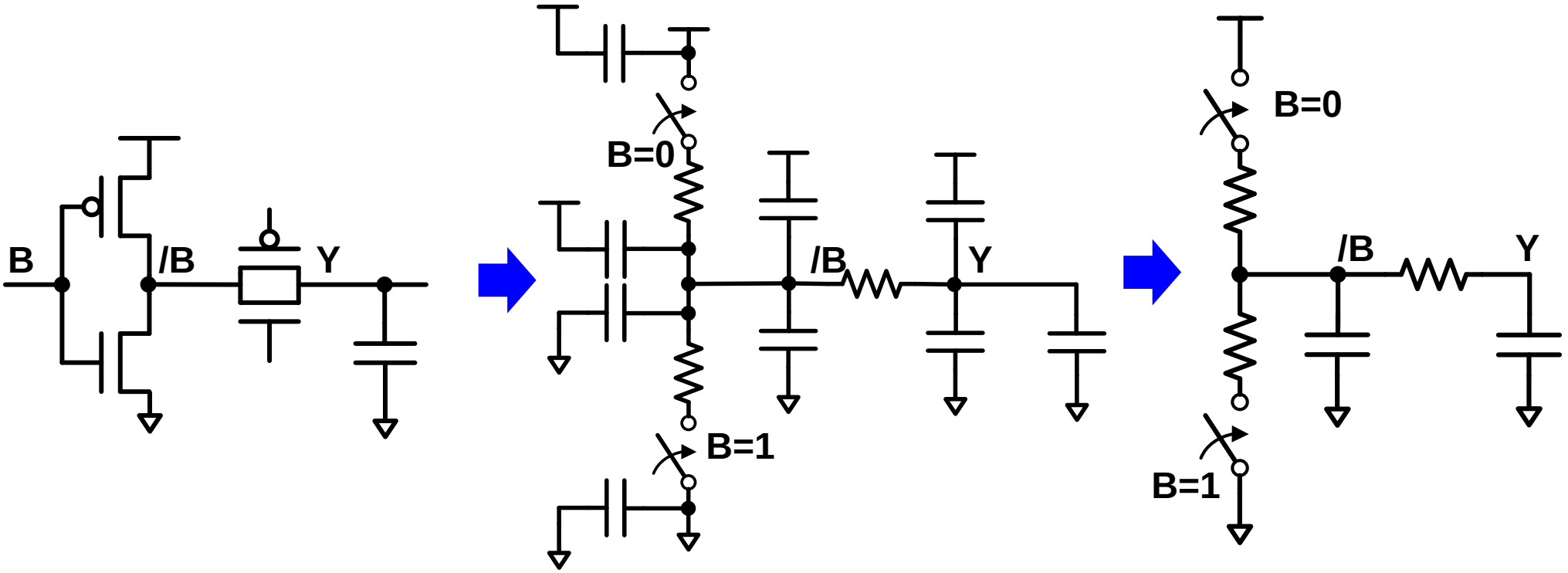
RC Tree Representation for CMOS Inverter

- One transistor exists between signal node and power rail.

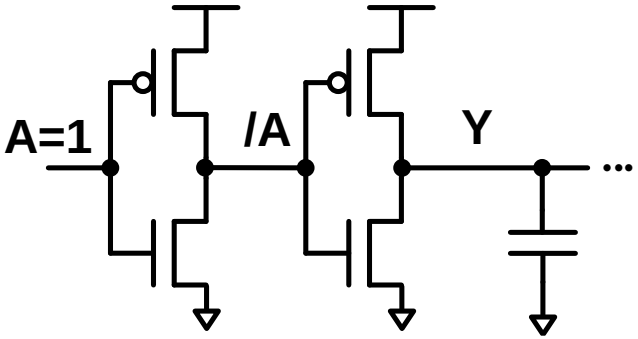


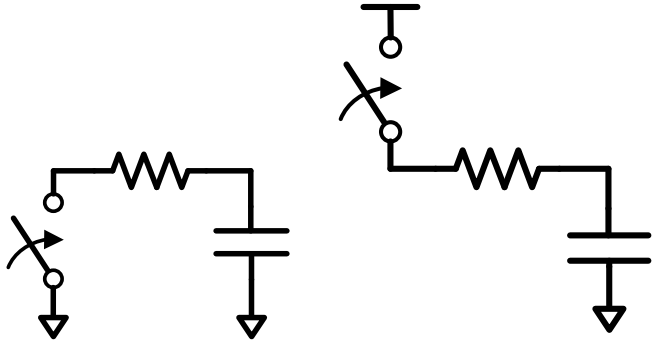
RC Tree for Transmission Gate or Pass Transistor

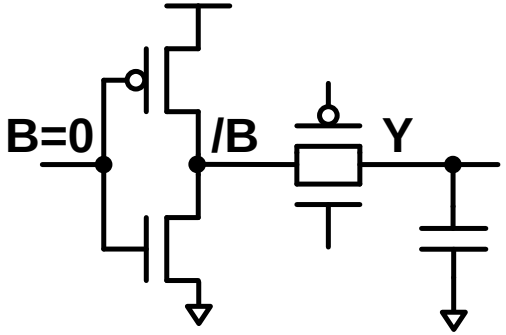
- Additional “R” exists between signal node and power rail.

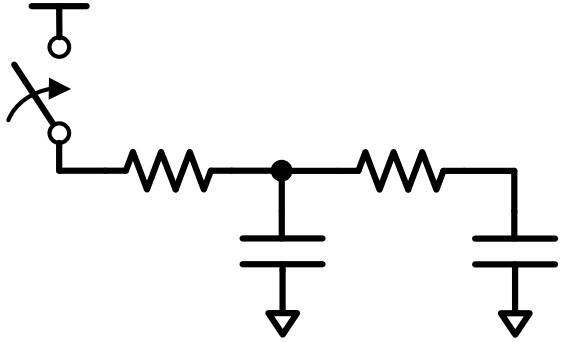


Inverter vs. TG



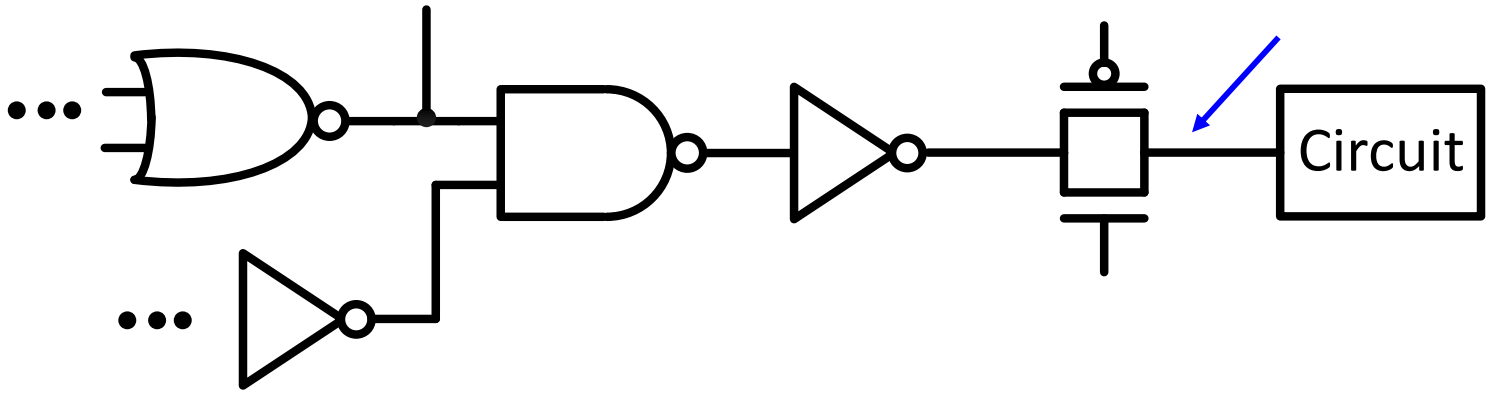






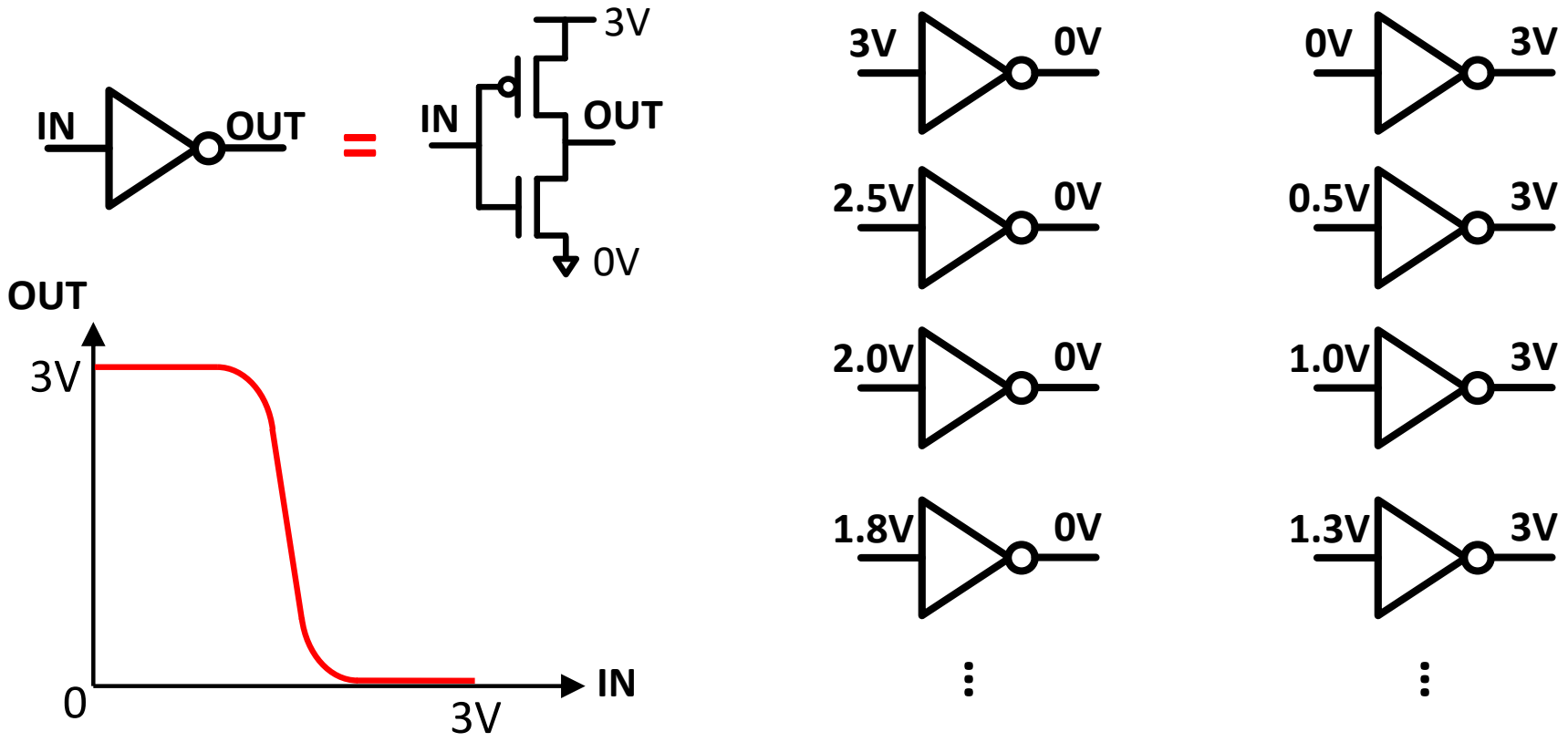
Effect of
Path Connected w/ Transmission Gate

- It increases the effective resistance of the path to power rail.
- What if the cap of the driven node is very large?



Restoring Feature of Inverter

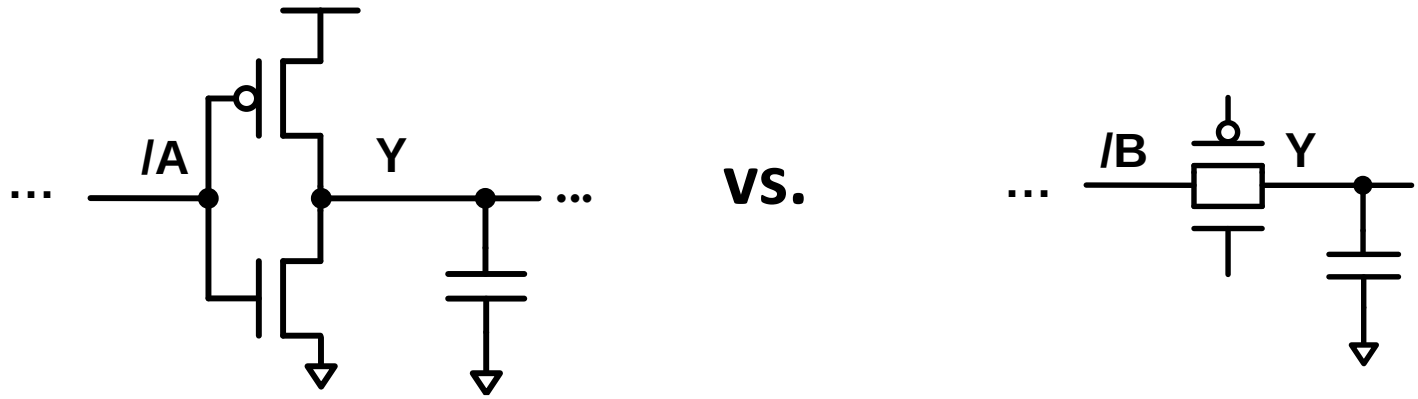
- When V_{DD} = 3V, how would the output of the inverter be **at the steady state (=infinite time is passed)**?



➔ **We can say a signal is restored in the CMOS inverter**

Noise Sensitivity

- Suppose /A or /B is shocked by the noise. How would Y be?
- Sometimes, it is said as you should avoid the diffusion input.

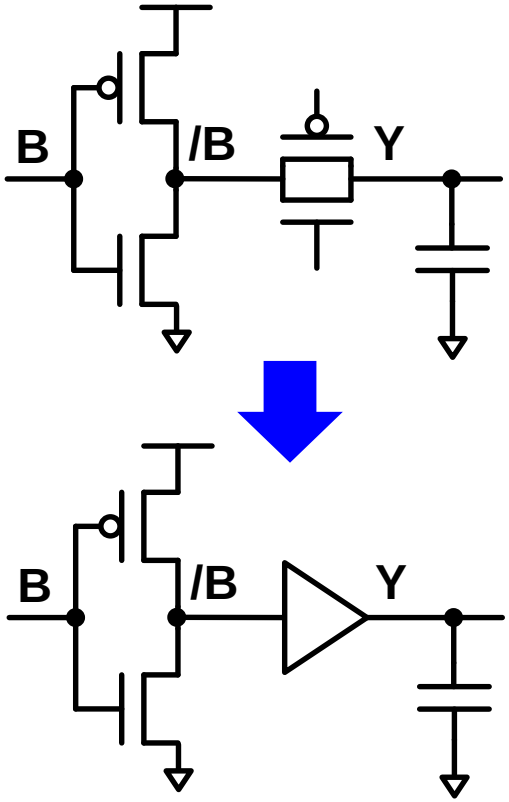


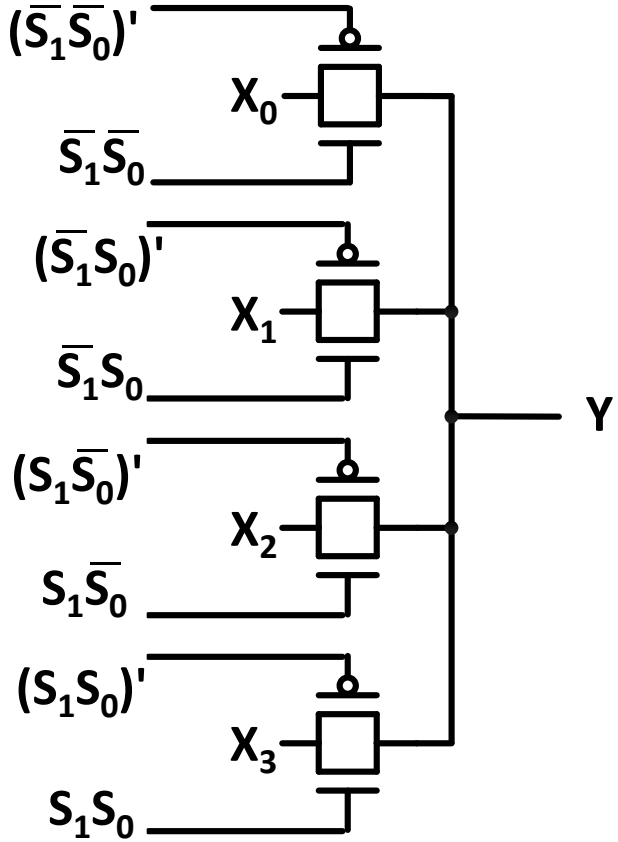
How Can We Mitigate Speed & Noise Issue in TG?

- ✓ Defining tri-state
- ✓ Tristate inverter design

Can't We Use Buffer Instead?

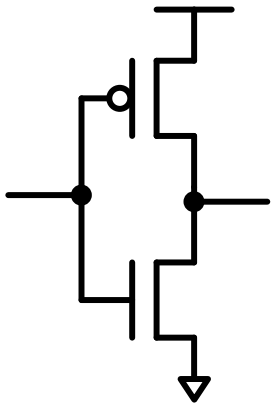
- Buffer has the restoring capability.
- **NO! It can't disconnect the path. Think of MUX example!**



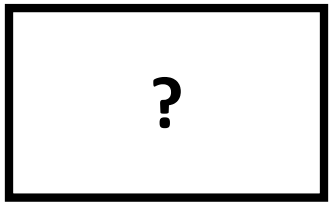


What We Need is

- Buffer is nothing but 2 stage inverters; we can focus on the inverter.
- What we need an inverter that can yield three states



A	Y
0	1
1	0

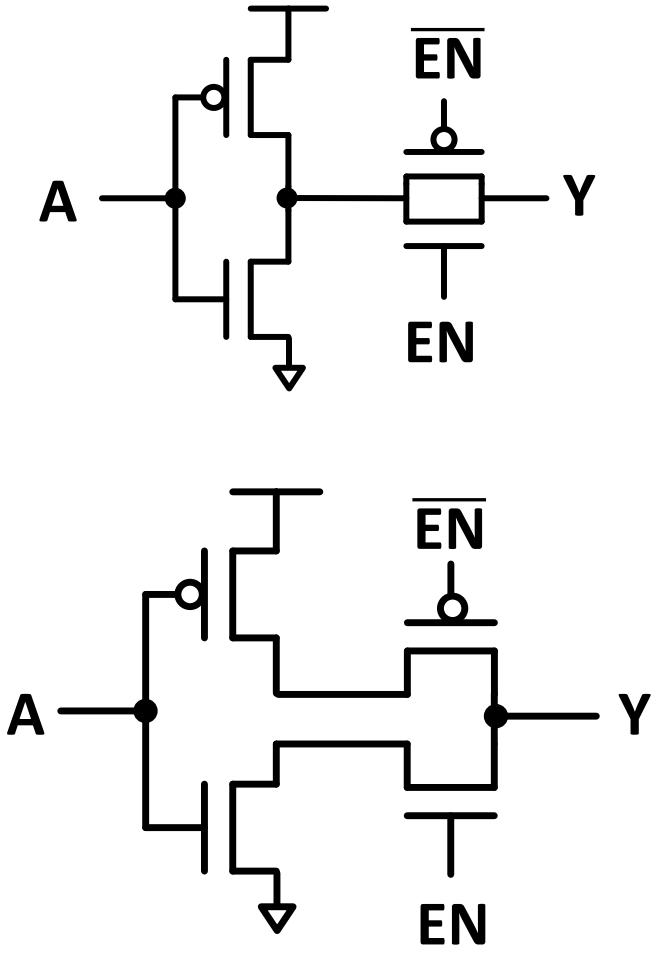


EN	A	Y
0	0	Disconnected
0	1	Disconnected
1	0	1
1	1	0

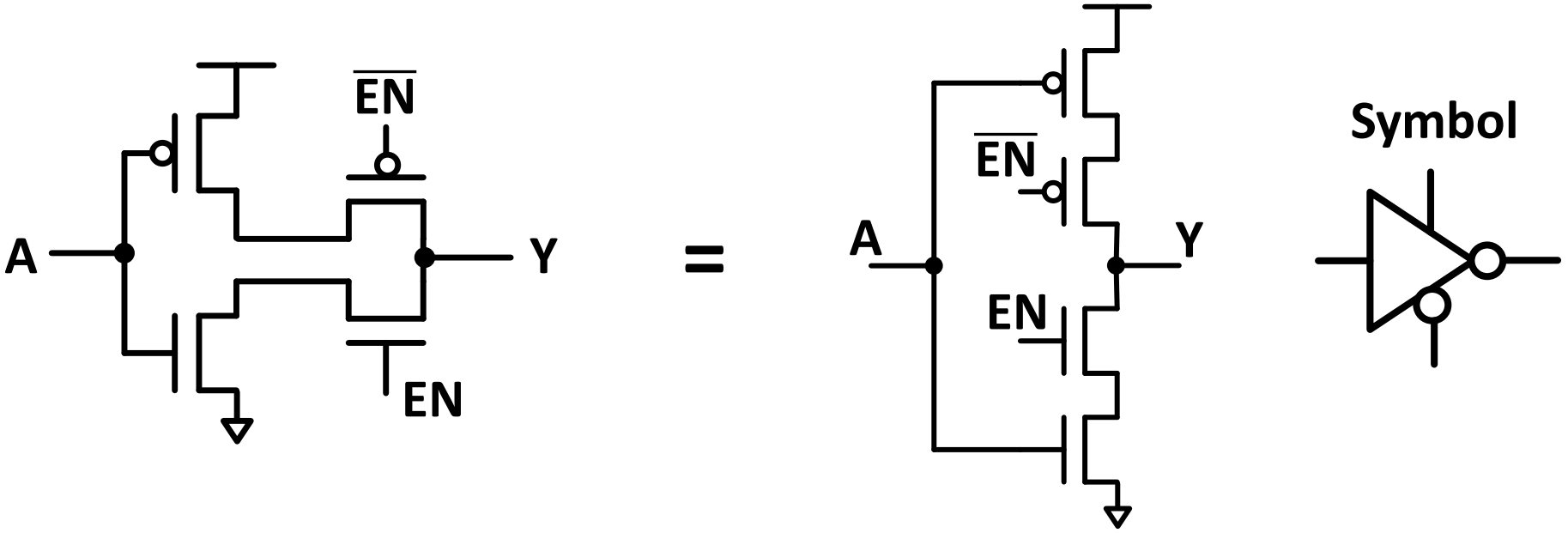
Normally Being an Inverter but Disconnected when EN = 0

- You can start from the inverter

EN	A	Y
0	0	Disconnected
0	1	Disconnected
1	0	1
1	1	0



Tri-state Inverter

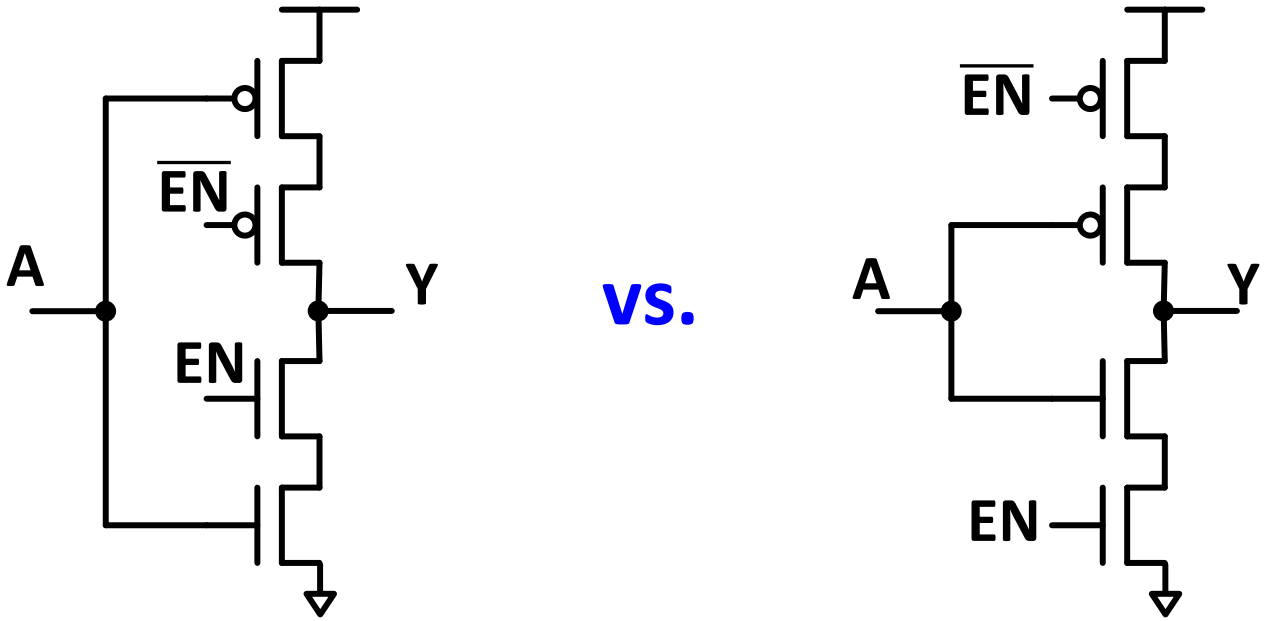


EN	A	Y
0	0	Disconnected Z
0	1	Disconnected Z
1	0	1
1	1	0

EN	Y
0	Z
1	/A

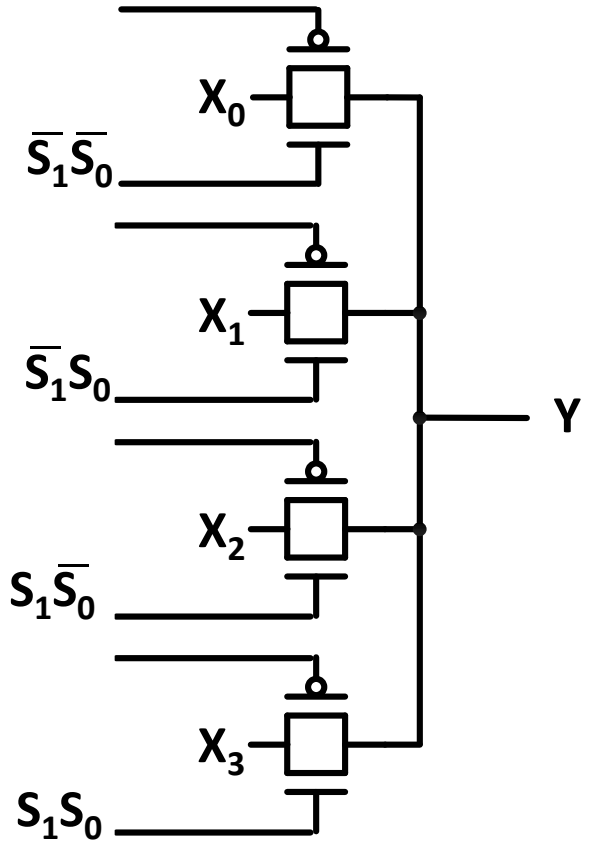
How About This?

- If the output is tristated but A toggles, charge from the internal nodes may disturb the floating output node.



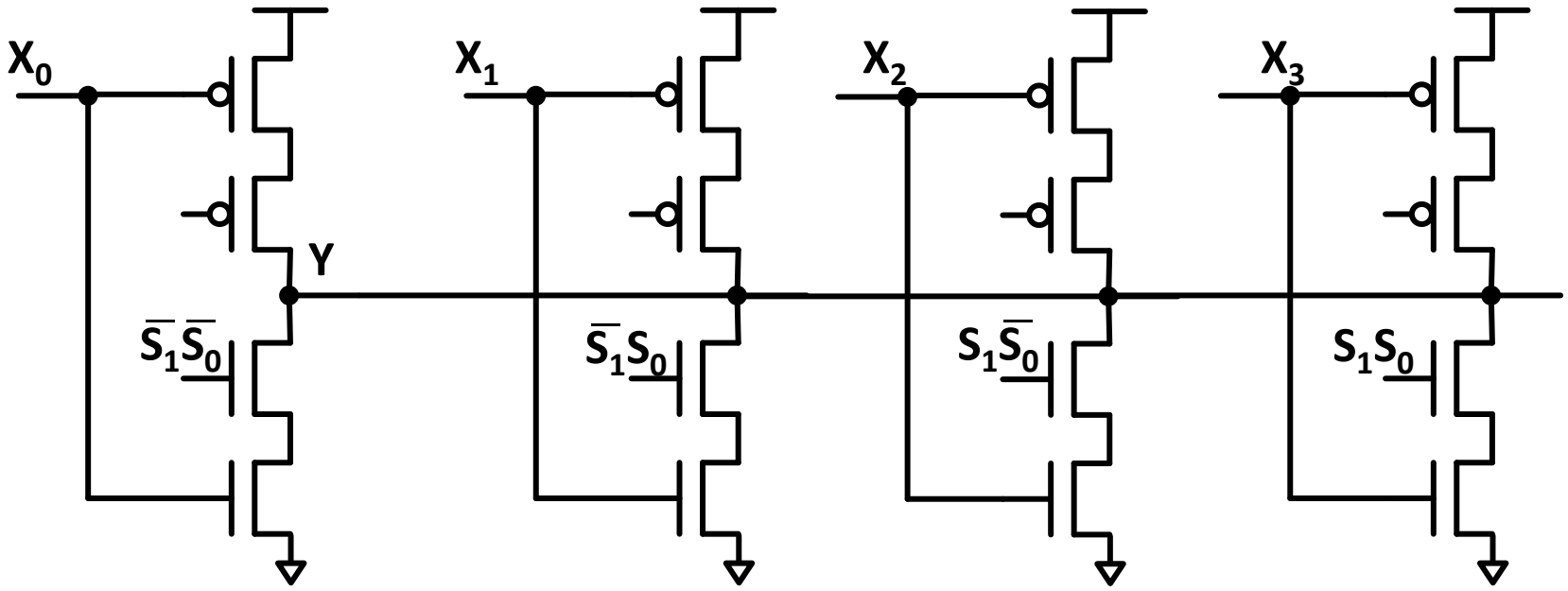
Revisit the TG based 4:1 MUX

- (PMOS control signals is not shown)



Tri-state Inverter based 4:1 MUX

- (Again, pMOS control signals is not shown)



What We Have Learned

- ✓ How switch can be implemented ➔ Pass TR vs. TG
- ✓ TG operation its application (MUX) ➔ Key is to disconnect
- ✓ Speed and Noise issue in TG ➔ Tri-state inverter