Logic Circuit Families (2)

Hanwool Jeong

hwjeong@kw.ac.kr

Contents

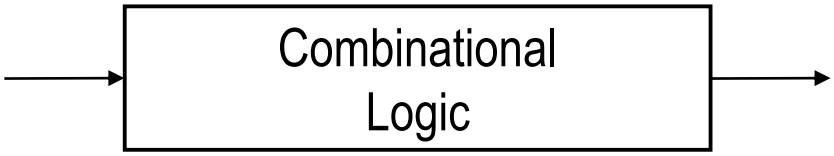
- Pseudo nMOS
- Cascode Voltage Switch Logic
- **Dynamic Circuit and Domino Logic**
- Pass-Transistor Circuits

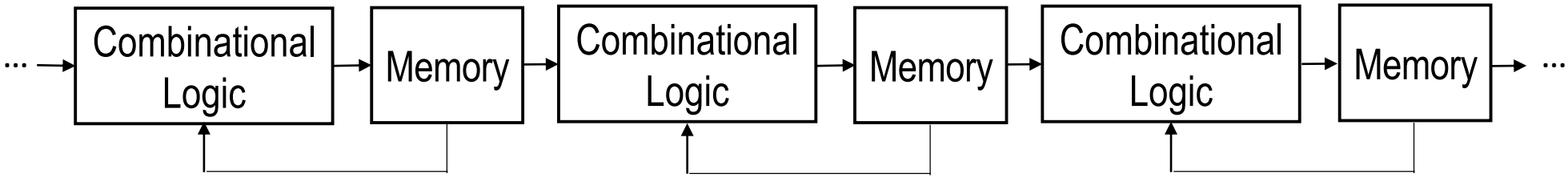
Dynamic Circuit and Domino Logic

- ✓ Replacing always-pull-up of pseudo nMOS with “clocked” pull-up

Combinational Circuits vs. Sequential Circuits

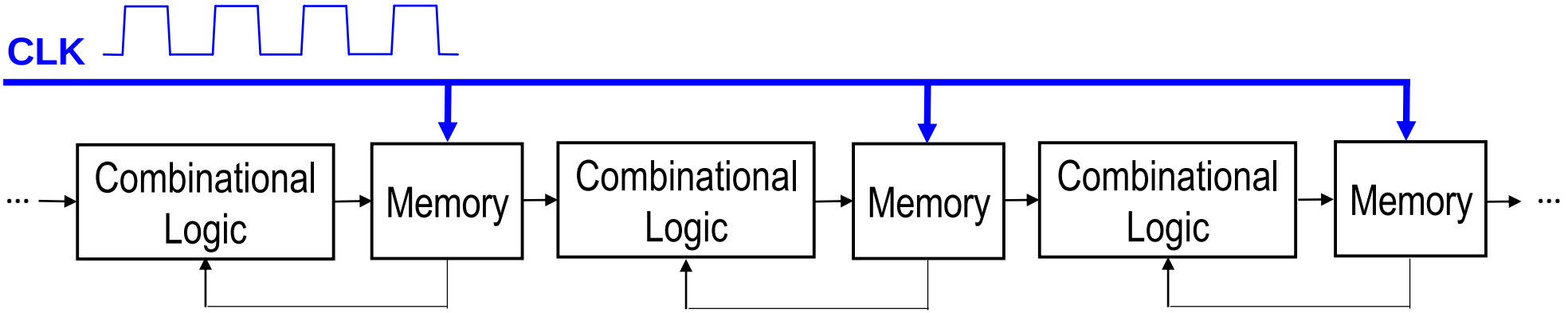
- Combinational circuit: output is a function of the current inputs.
- Sequential circuit: output depends on **previous** as well as **current** inputs; such circuits are said to have state.
- Sequential logic is essential for today electronic system (Have you heard of pipeline or finite state machine?)





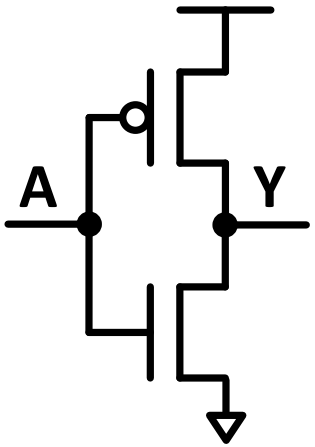
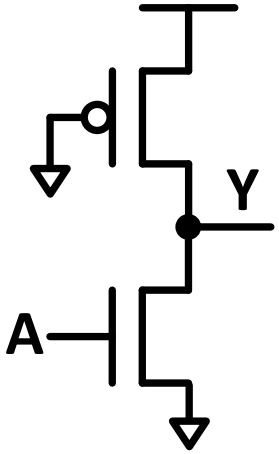
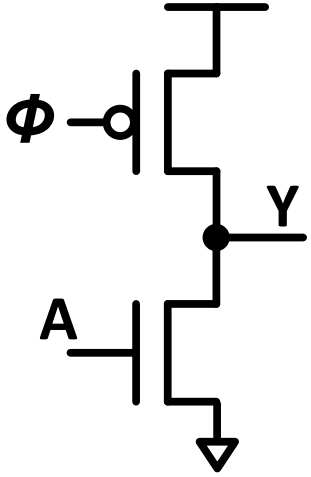
“Synchronous” Sequential Circuit

- The state of device changes only at discrete times dominated by a “clock” signal.

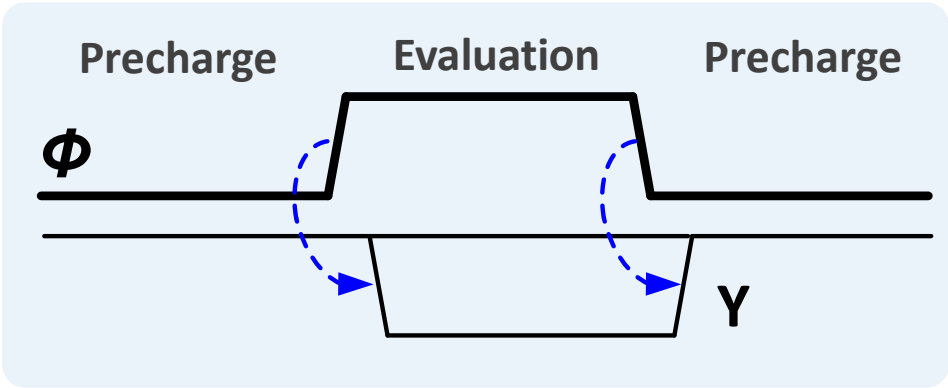


➔ Besides the main CLK signal, many other dynamically changing “control” signals can be generated

Dynamic Inverter Utilizing Clocked Pull-up

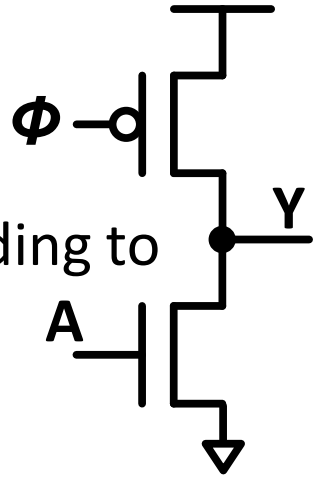
Static CMOS	Pseudo NMOS	Dynamic
		

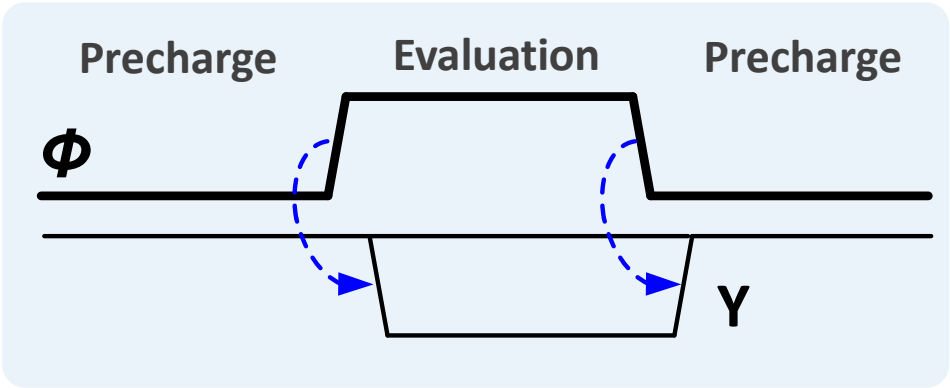
Operated in two phases:
1) Precharge and 2) Evaluation



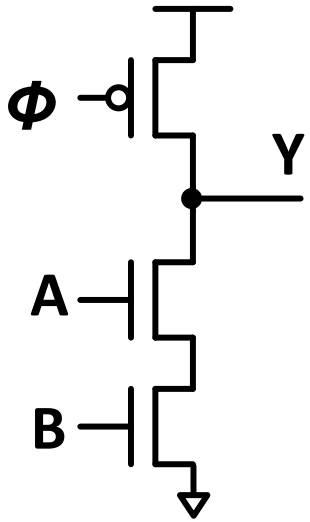
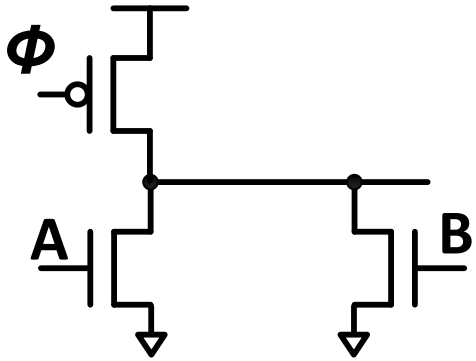
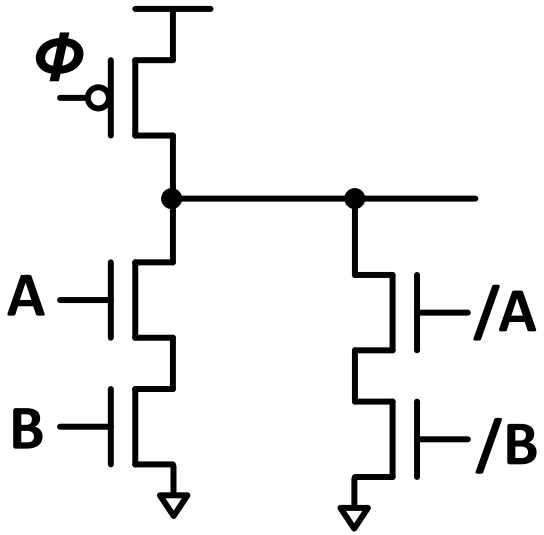
Dynamic Logic Gate

- Precharge (Φ=0)
  - Clocked pMOS is ON, initializing Y high.
- Evaluation (Φ=1)
  - Clocked pMOS is turned off
  - Y may remain high or e discharged low according to pulldown network controlled by inputs.
- Why is it faster than CMOS gate? Area?
- No static power as pseudo-nMOS.



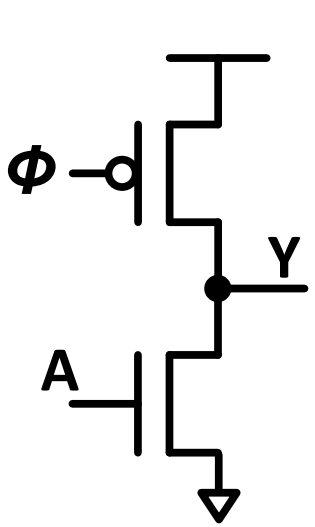


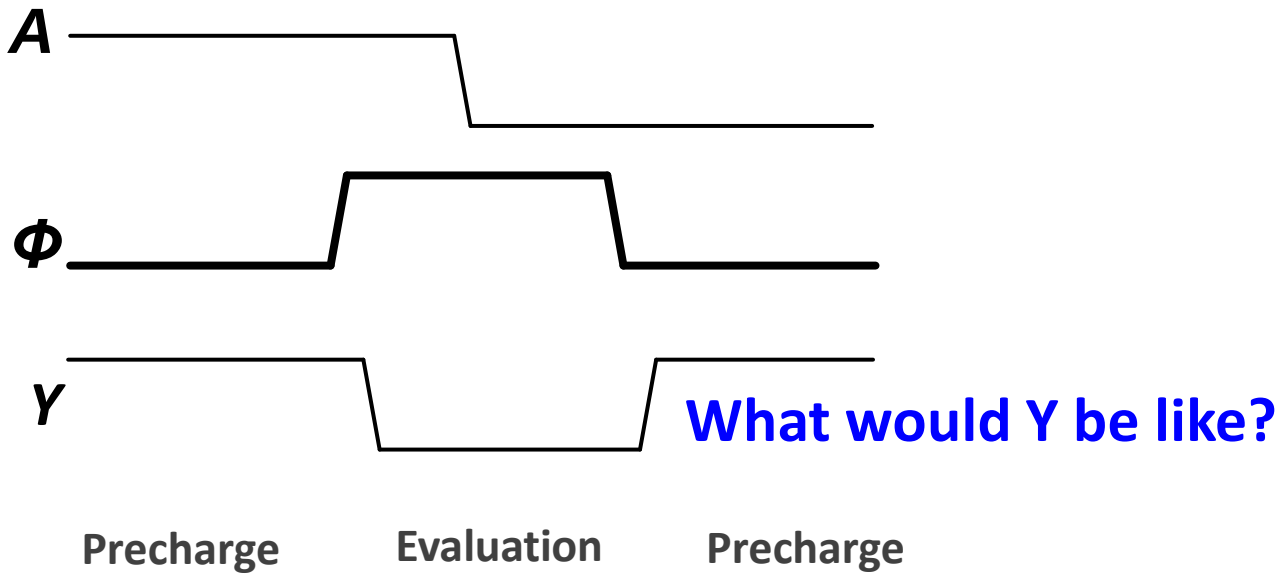
Various Dynamic Logic Gates

NAND2	NOR2	XOR2
		

Can You Find Potential Problems?

1) During precharge, there might be contention.
2) If A falls during evaluation, Y cannot be raised.
   (Monotonically falling output, monotonicity problem)



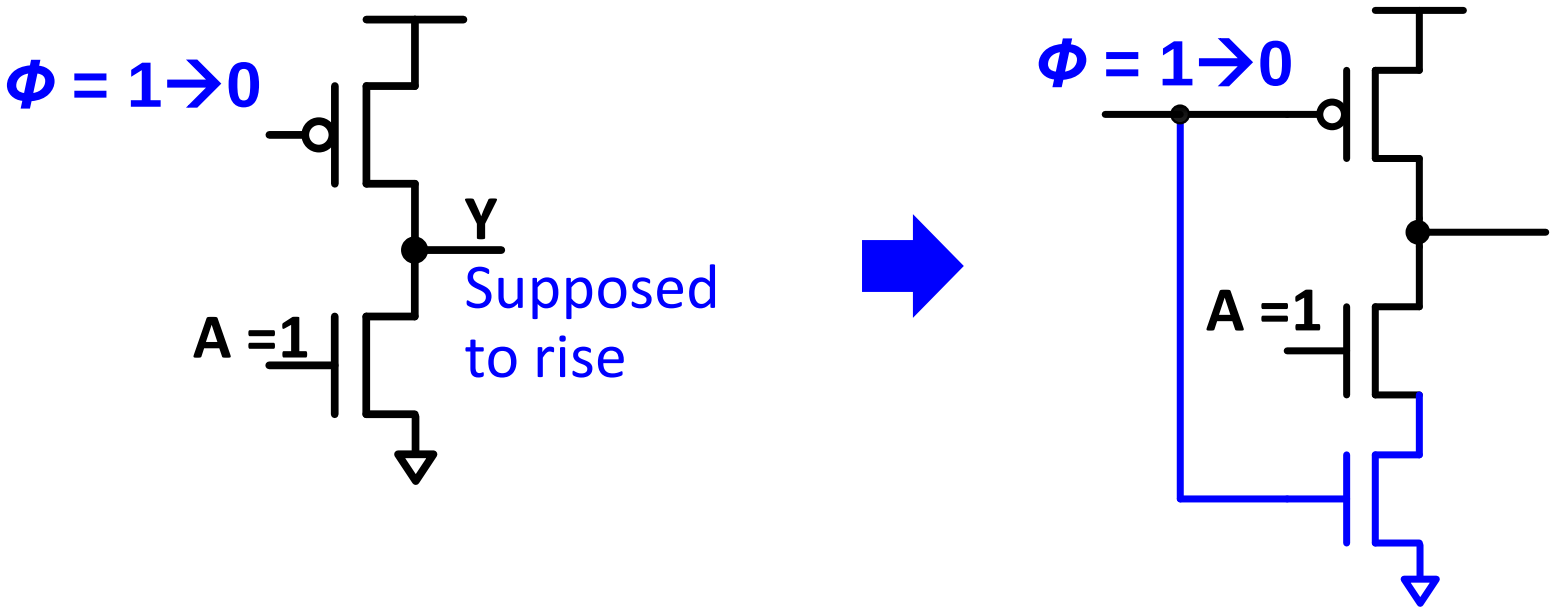


How Can You Resolve Contention Problem?

- State your goal verbally and specifically.

  "When Φ = 0, the pull-down network should be disabled."

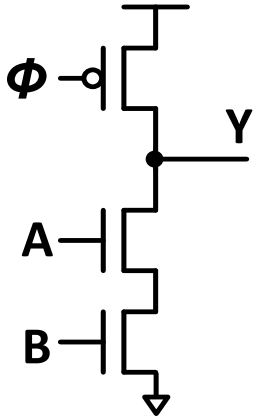
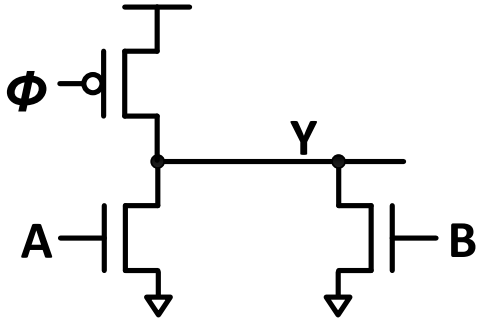
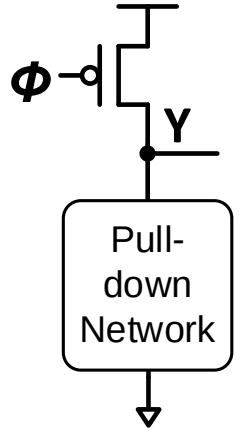
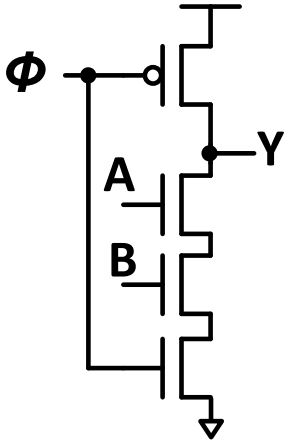
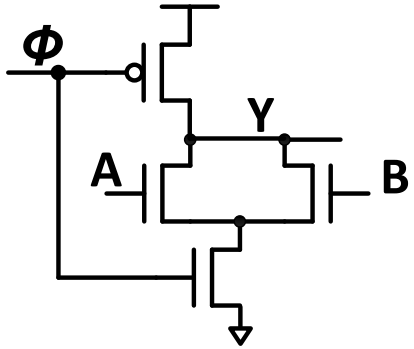
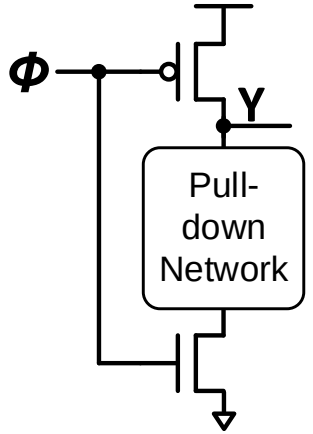
Condition : MOSFET gate node **Operation : MOSFET drain current**



Footed Dynamic Inverter

Footed Dynamic Gates

- Width needs to be increased to achieve equal speed

	NAND2	NOR2	General logic
Unfooted			
Footed			

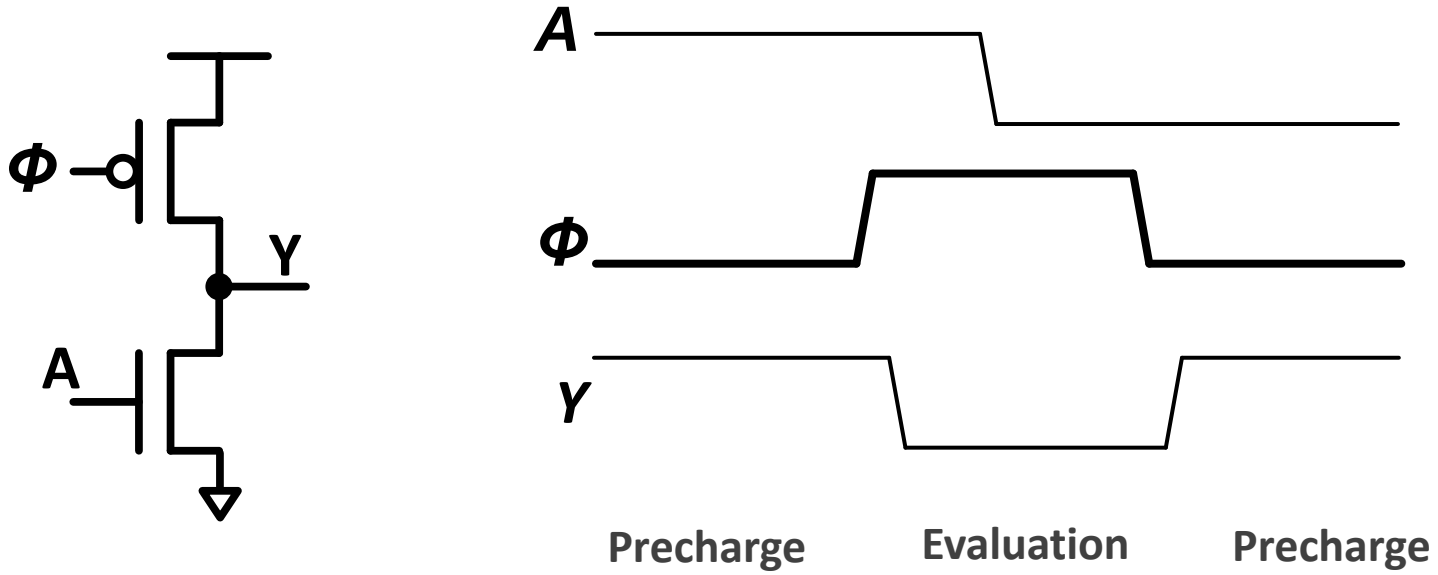
How Can You Handle Monotonicity Problem?

- What is the cause of the problem?

➔ ***A*** falls during the evaluation.

➔Can't we force ***A*** only to **rise** or **kept low** during evaluation?

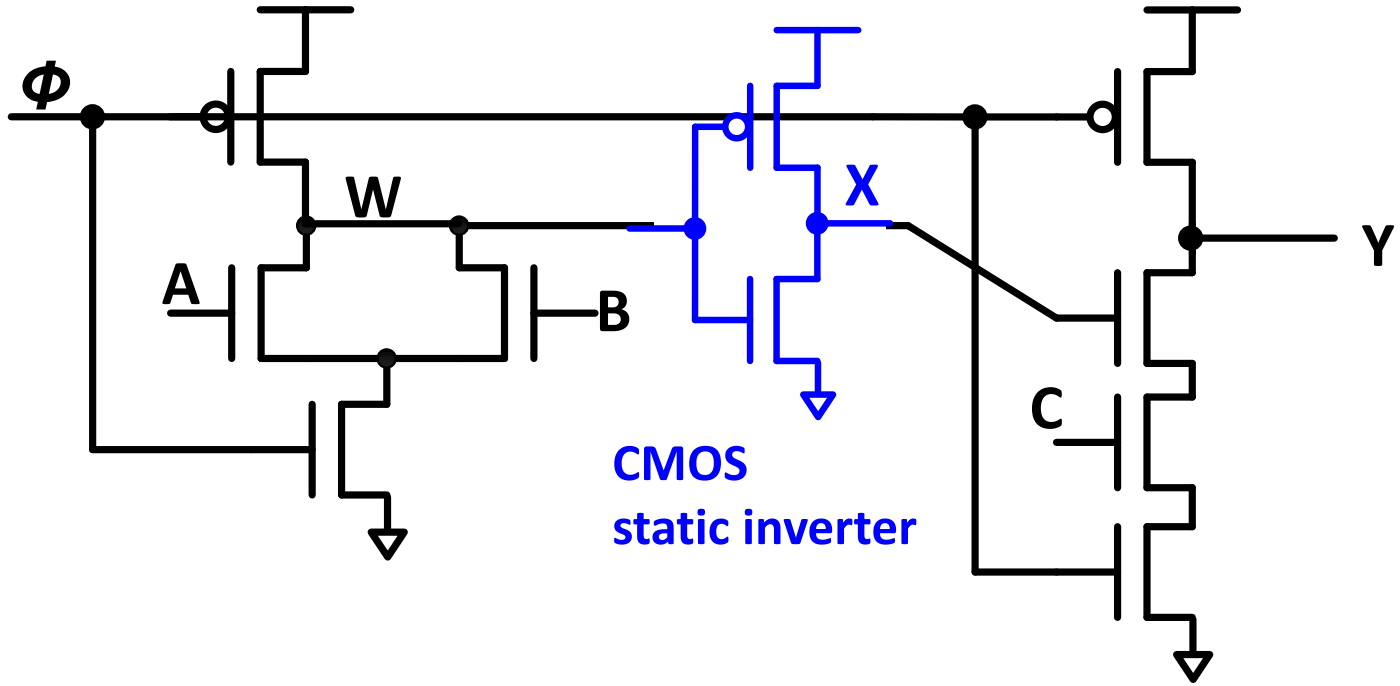
➔Can't we make ***A*** **monotonically rising** during evaluation?



How Can We Achieve an Input "Monotonically Rising" During Evaluation

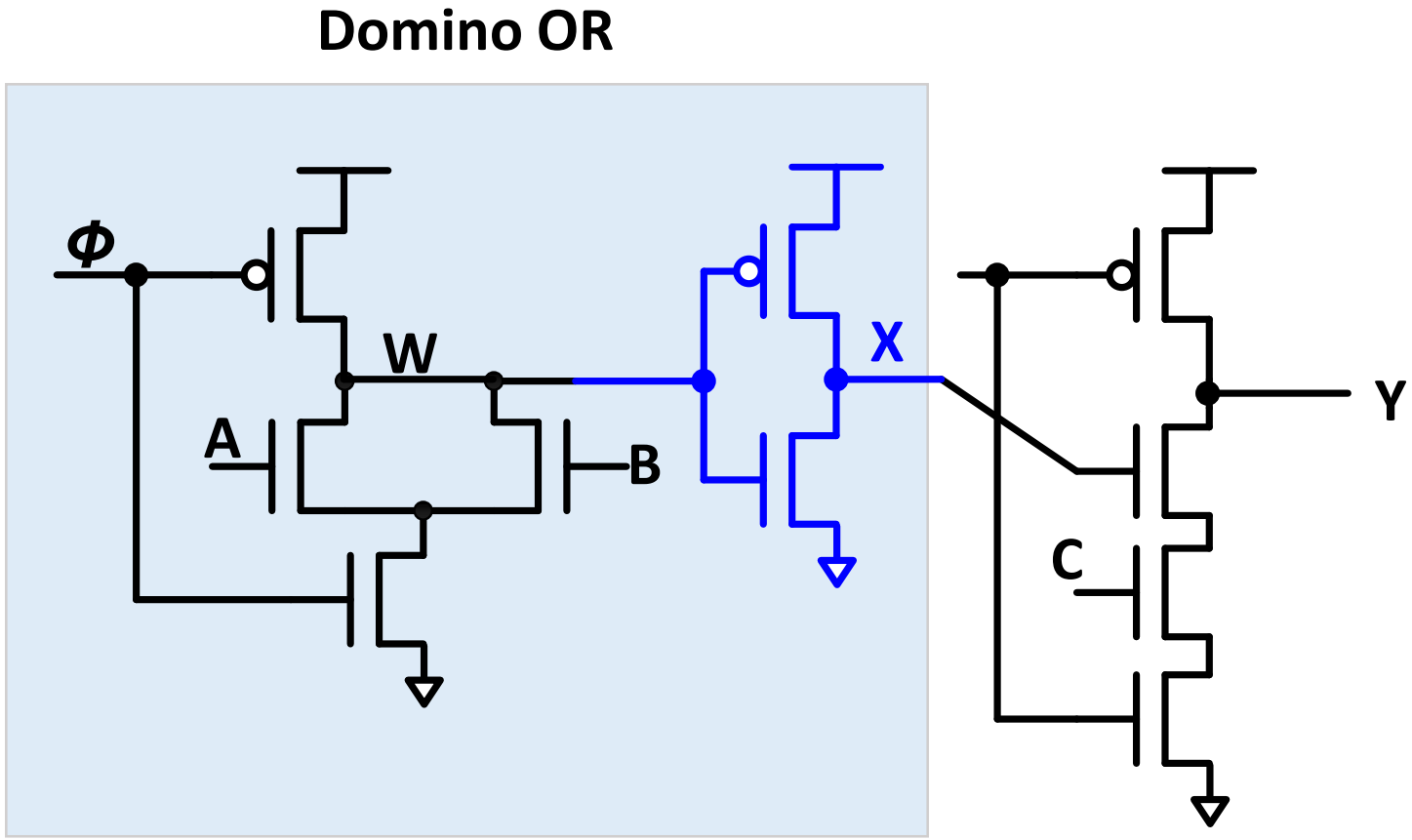
- Dynamic gate output is **monotonically falling** during evaluation

➔ Then, we can easily achieve a signal monotonically rising during evaluation by



Domino Logic Gate

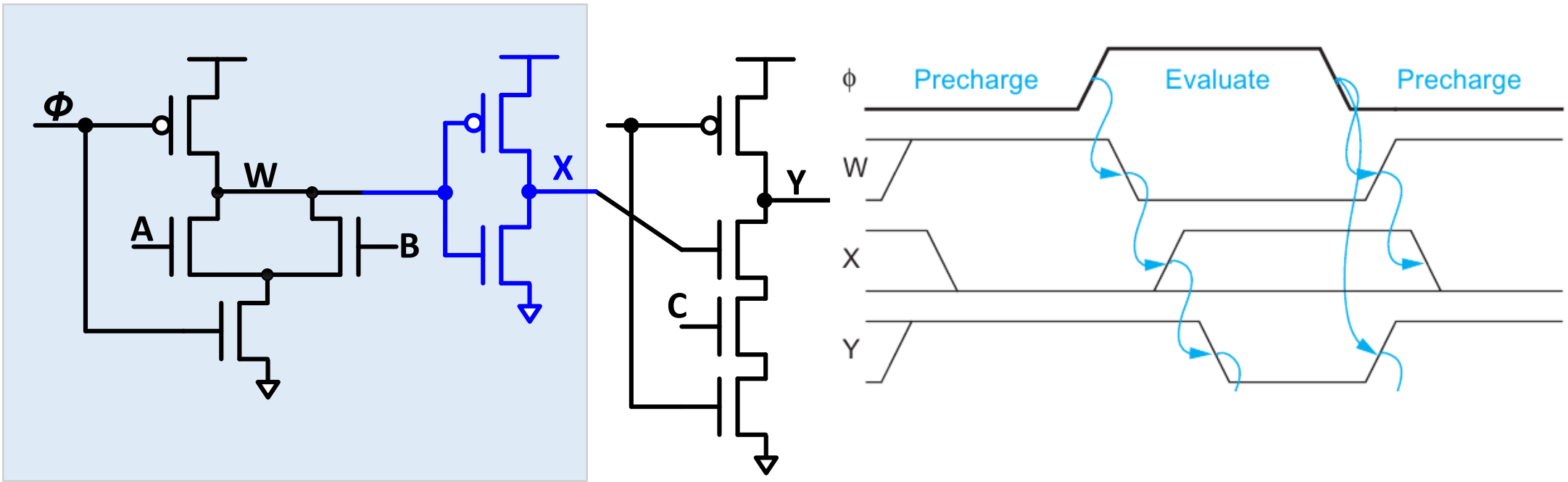
- Domino logic = Dynamic gate + static inverter



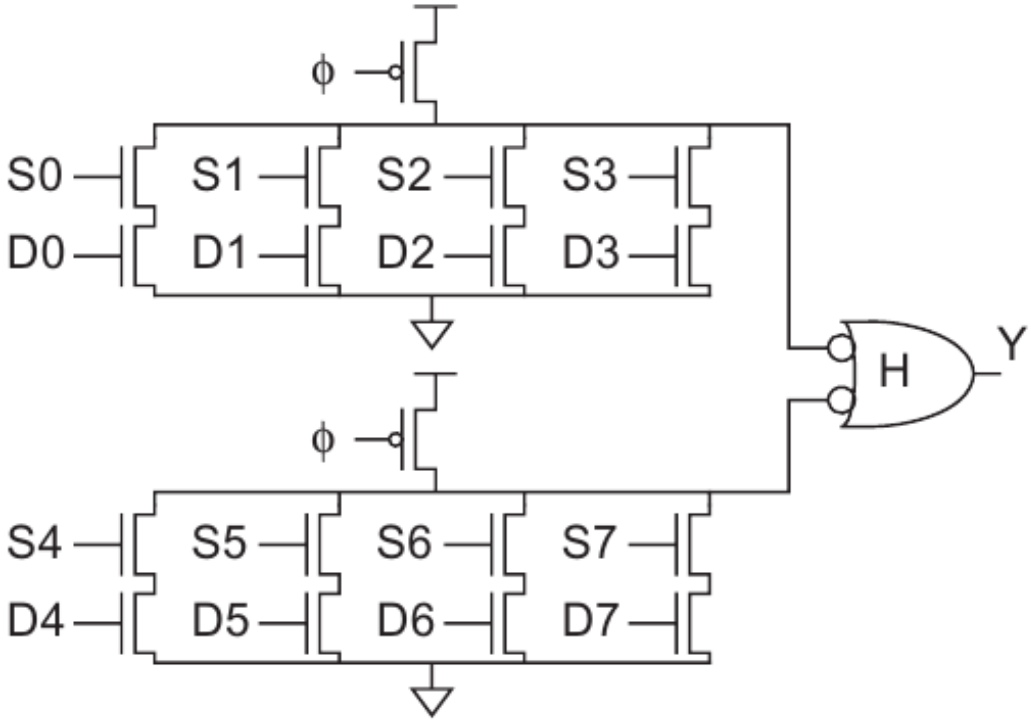
Operational Waveform

- Monotonicity problem is solved

Domino OR



8:1 MUX Using Domino Logic

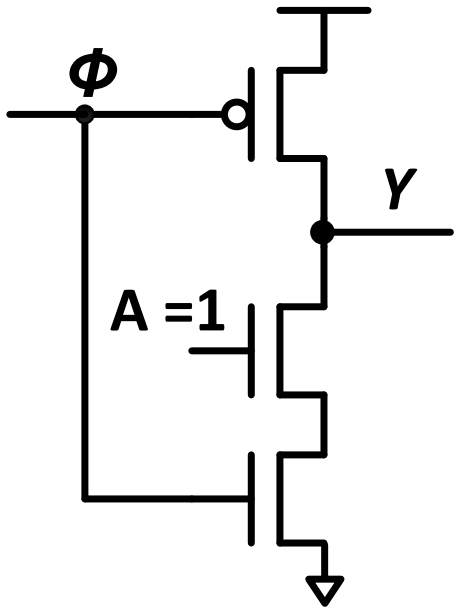


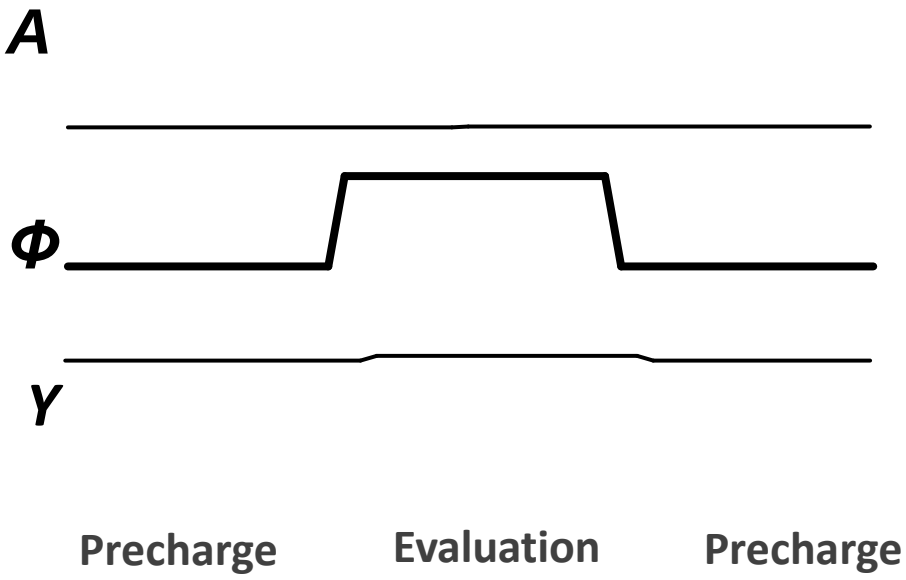
Potential Problem for A = 0

3) When A = 0, Y is floating high.

➔**"When Y is high, Y should be driven to V_{DD}."**

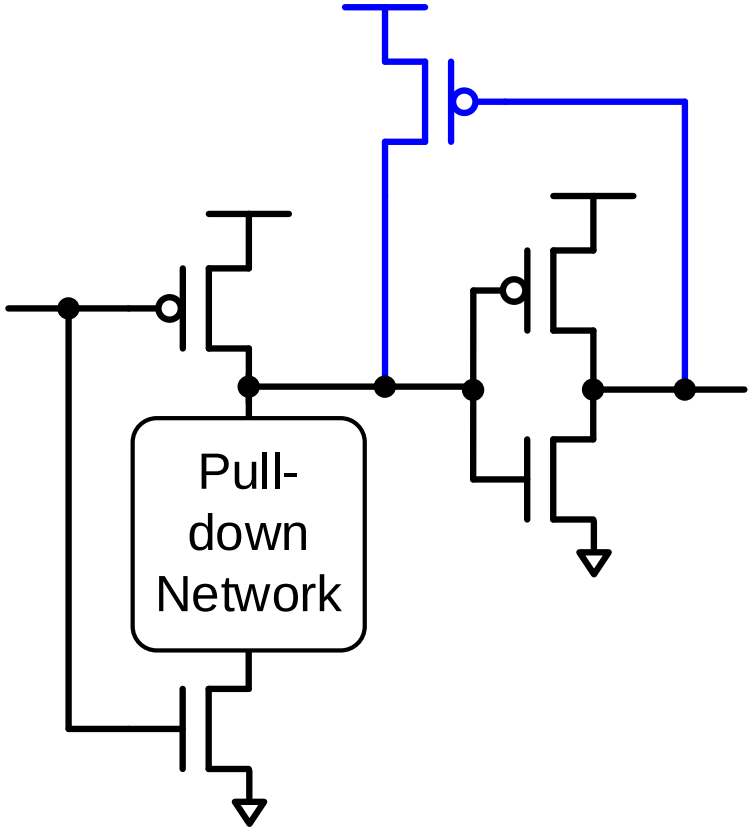
➔**Who can drive Y to V_{DD}?**





Keeper Implementation for Noise Robustness

- Note that keeper pMOS should be sufficiently weak.



Summary

- Clocked pull-up + pull-down network for logic implementation
- Contention during precharge can be solved through footed circuit
- Monotonicity problem is resolved by domino logic
- Keeper can be utilized to prevent output floating of the dynamic gate, but the strength should be carefully determined.