Chap 6 (4)

Synchronous Counter;

Up/Down Binary Counter & BCD Counter

Hanwool Jeong

hwjeong@kw.ac.kr

What Should We Bear in Mind?

- Up/Down binary counter
  - Should be able to select mode, and operation should be changed up to the selected mode.
- BCD Counter
  - Because of the return to 0 after 9, a BCD counter does not have a regular pattern, unlike a straight binary count.

Present State				Next State			
Q_8	Q_4	Q_2	Q_1	Q_8	Q_4	Q_2	Q_1
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0

Mode Signal Specification
Up-Down Binary Counter

- Let's design an up-down counter operating according to user choice. **What do we need for inputs?**

Up	Down	Operate
0	0	
0	1	
1	0	
1	1	

- We should select "prior" mode input,
- And take it into consideration during the circuit design phase.

Start to Design Up-Down Binary Counter; Down Mode Respect

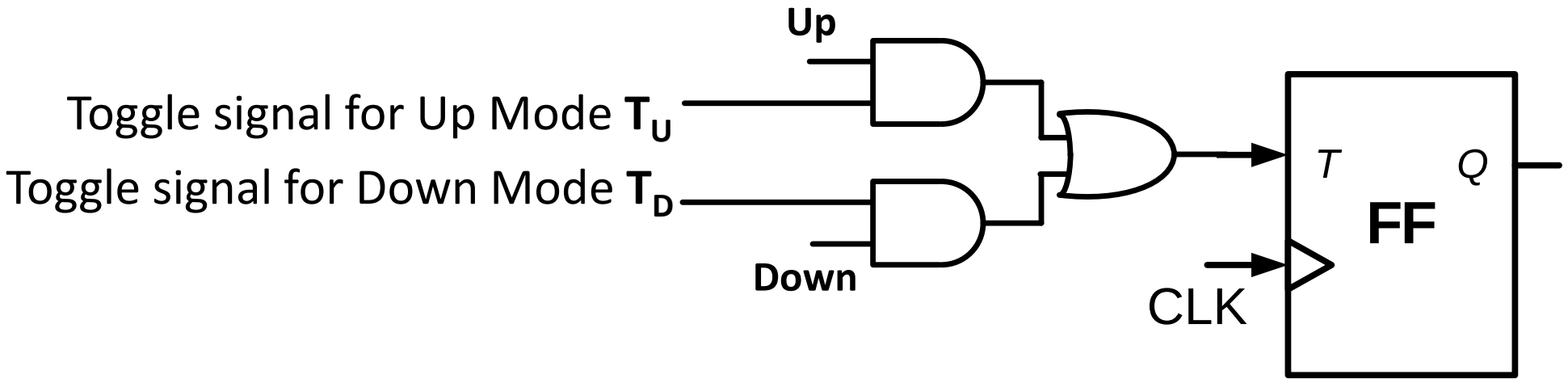
- Revisit how we do for typical up binary counter
- For now, we focus how it should be for “down” mode.
  - A_0 is complemented with each pulse.
  - A_1 is complemented when $A_0 = 0$.
  - A_2 is complemented when $A_1A_0 = 00$.



A_3	A_2	A_1	A_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0

We Can Diversify Up/Down Modes by

- For now, we use T-FF



- Is this all? Verify it with the mode signal table:

Up	Down	Operate
0	**0**	Hold
0	**1**	Down
1	**0**	Up
1	**1**	Up

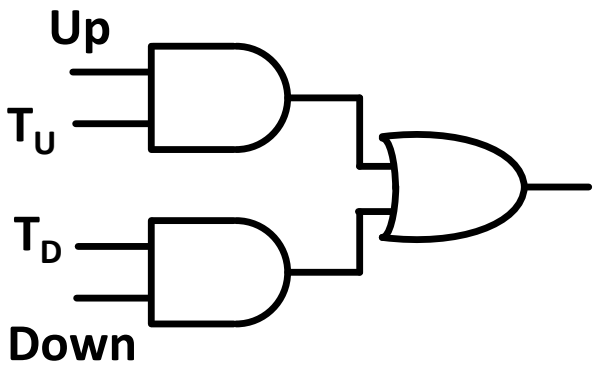
How can we realize the priority?

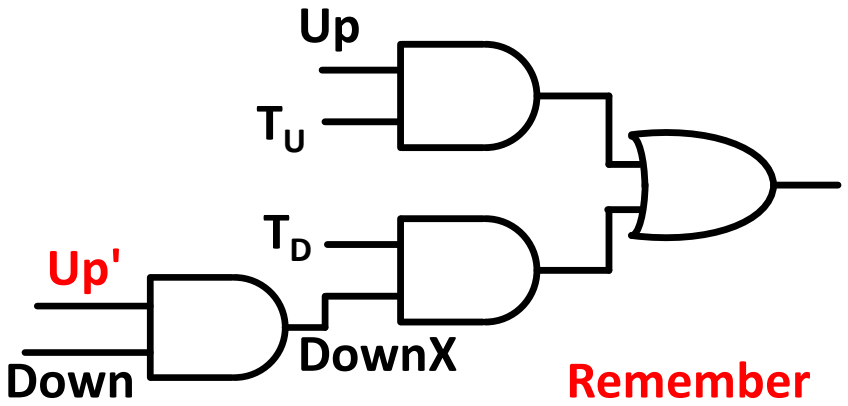
Considering Priority

- When up, down = (1,1), T_U must be passed.

➔**Although down is 1, it would be valuable only when up = 0**

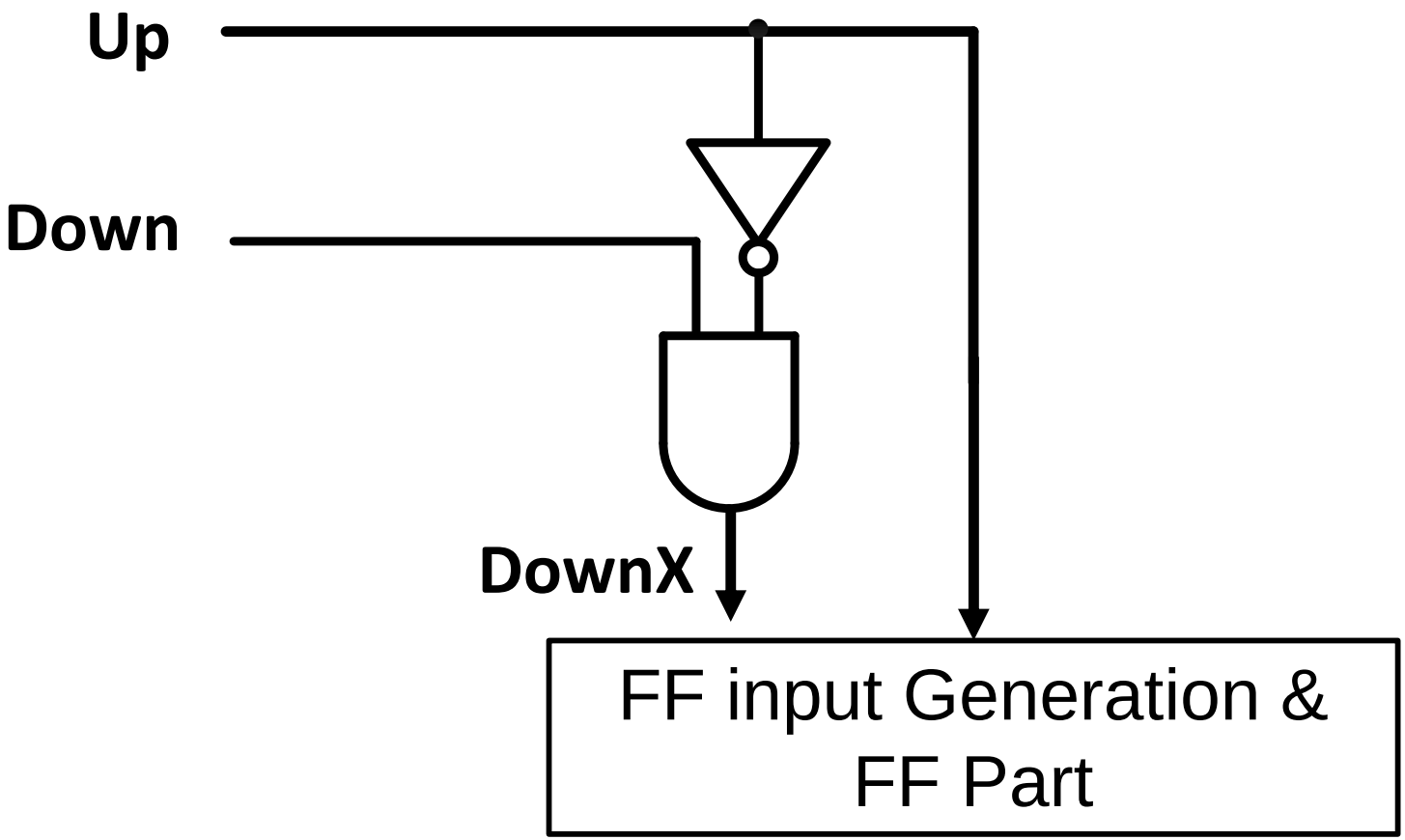
➔**Although down is 1, it would be disabled when up = 1**





Remember
DownX & Up
Cannot be 1
At the same time

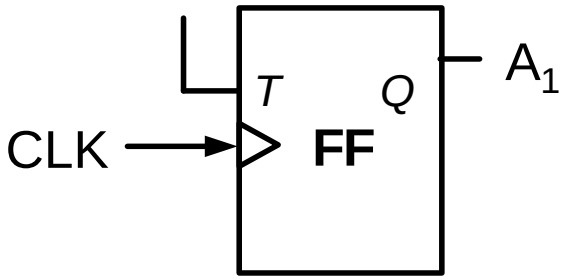
Mode Selection Signal Considering Priority



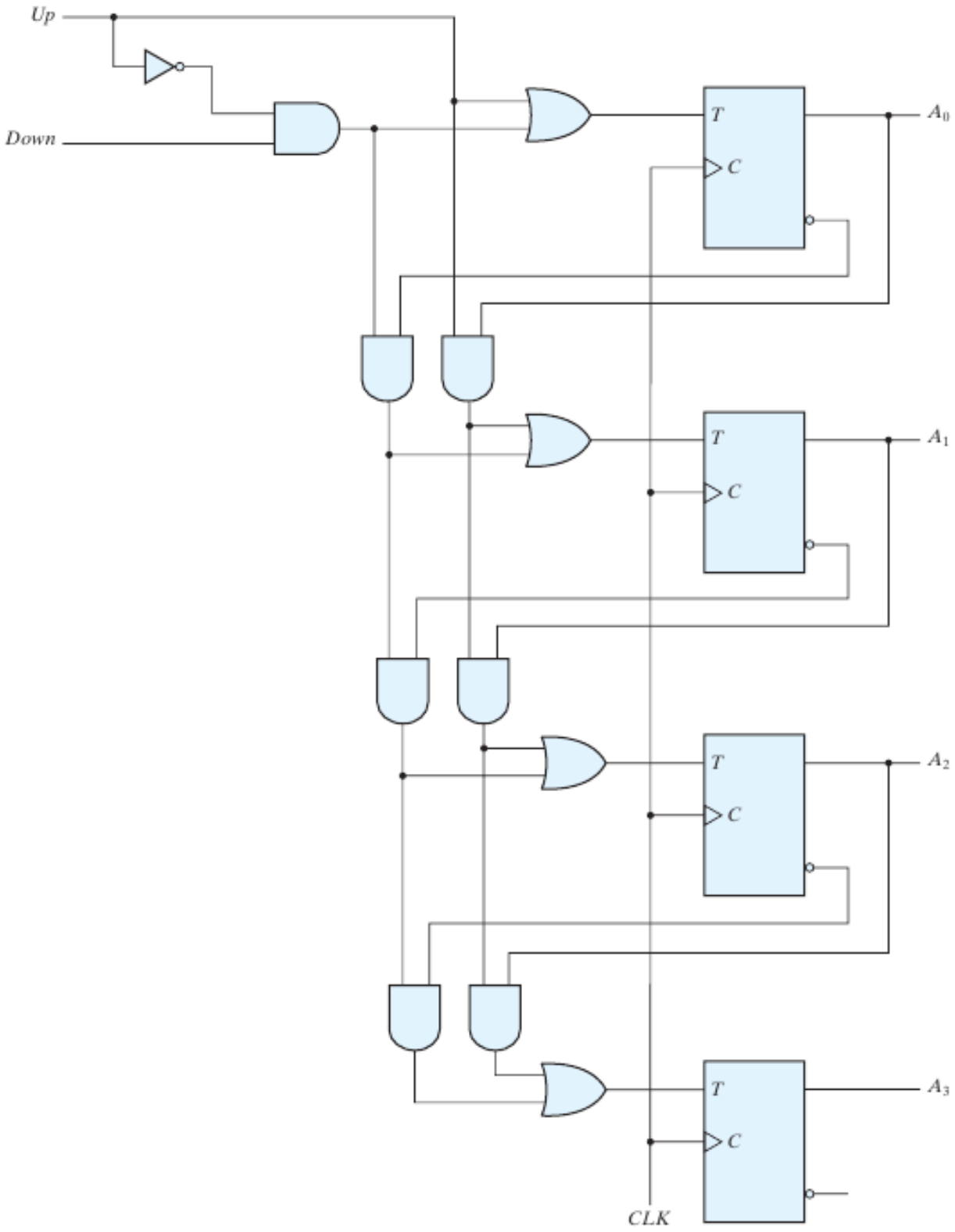
Bit-by-Bit Design for Binary Counter

- Now we focus on **"FF input generation"** – that is, T_U & T_D.

	T_U	T_D
T-FF for A_0	Every clk edge	Every clk edge
T-FF for A_1	clk edge when A_0=1	clk edge when A_0=0
T-FF for A_2	clk edge when A_1A_0=11	clk edge when A_1A_0=00
….	….	….



A_3	A_2	A_1	A_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0


Up
Down
T
C
A_0
T
C
A_1
T
C
A_2
T
C
A_3
CLK

You Remember Synthesis Procedure?
Designing Synchronous Sequential Circuit

- We have the slide learned :

What We Have Learned

- How to design a sequential circuit
- **State (transition) table**
- Current input & state ➔ Output & Next state
  - Here, FFs are used to store/update states
  - So, we need next state vs. FF input relationship
- **FF input table & FF input equations** can be obtained using **FF excitation table**
- Then you can finalize the circuit design
- **State diagram** is more intuitive way to express circuit operation and better starting point of circuit design!

State Transition Table Approach

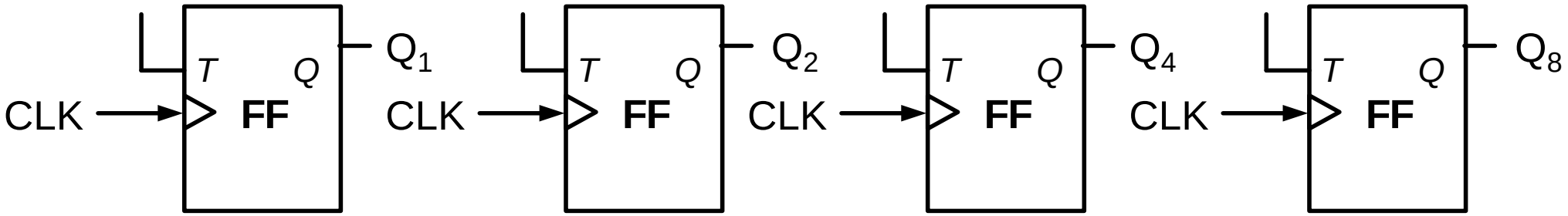
Present state				Next state				Output	FF Inputs			
A_3	A_2	A_1	A_0	A_3	A_2	A_1	A_0	Y	T_3	T_2	T_1	T_0
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1
0	1	0	1	0	1	1	0	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	1	0	1	0	0	0	0	1	1
1	0	1	0	1	0	1	1	0	0	0	0	1
1	0	1	1	1	1	0	0	0	0	1	1	1
1	1	0	0	1	1	0	1	0	0	0	0	1
1	1	0	1	1	1	1	0	0	0	0	1	1
1	1	1	0	1	1	1	1	0	0	0	0	1
1	1	1	1	0	0	0	0	1	1	0	1	1

BCD Counter

- binary-coded decimal from 0000 to 1001 and back to 0000.

Present State				Next State			
Q_8	Q_4	Q_2	Q_1	Q_8	Q_4	Q_2	Q_1
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0

$$T_{Q1} = 1$$
$$T_{Q2} = Q'_8 Q_1$$
$$T_{Q4} = Q_2 Q_1$$
$$T_{Q8} = Q_8 Q_1 + Q_4 Q_2 Q_1$$
$$y = Q_8 Q_1$$



Checkpoints

- ✓Mode selection
- ✓Priority consideration
- ✓State transition table based general counter design ; BCD counter
- ✓Coming up next: Parallel loadable counter