Chap 7 (1)
Random Access Memory

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Introduction

- A memory unit is a device to which binary information is transferred for storage and from which information is retrieved when needed for processing.
- There are two types of memories: random-access memory (RAM) and read-only memory (ROM).
- RAM stores new information **for later use**, performing write & read operation
- ROM is a programmable logic device (PLD), performing only the read operation with programming operation.

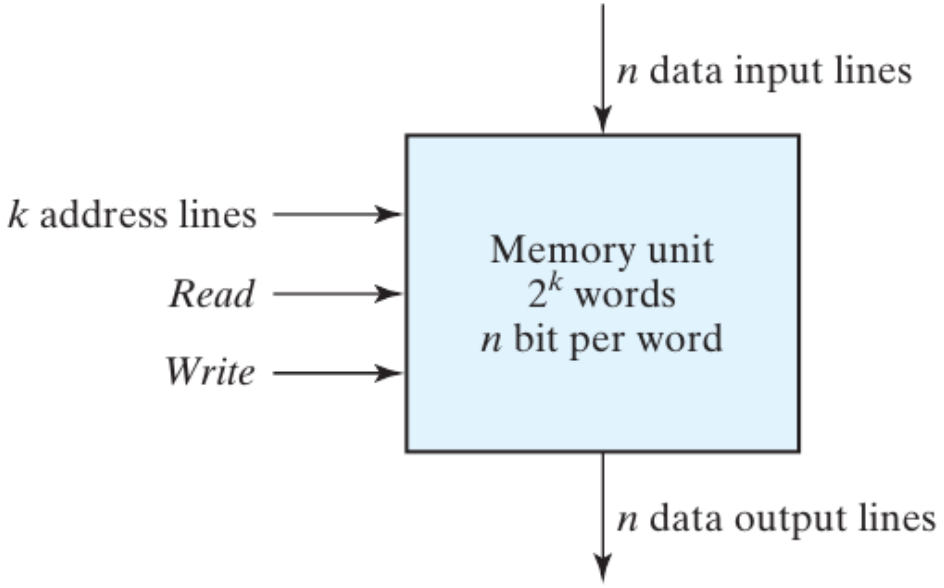
  ➔ Programming is a H/W procedure specifying the bits that are inserted into the hardware configuration of the device.

Various PLD

- A PLD is an integrated circuit with internal logic gates connected through electronic paths that behave similarly to fuses.
- In the original state of the device, all the fuses are intact.
- Programming the device involves blowing those fuses along the paths that must be removed in order to obtain the particular configuration of the desired logic function.
- ROM is one example of a PLD. Other such units are the programmable logic array (PLA), programmable array logic (PAL), and the field-programmable gate array (FPGA).

Random Access Memory & Requirement for Address Input

- RAM : The architecture of memory that information can be selectively retrieved from any of its internal locations
- Word : A group of bits that memory unit stores binary info.
- In most cases, words are multiples of 8 bits (=1byte) in length.



1024 words
= 1024 × 32bit

512 words
= 512 × 64bit

512 words
= 512 × 32bit

Memory Configuration Example

- 1K x 16bit memory:

Memory address		Memory content
Binary	Decimal	
0000000000	0	1011010101011101
0000000001	1	1010101110001001
0000000010	2	0000110101000110
⋮	⋮	⋮
1111111101	1021	1001110100010100
1111111110	1022	0000110100011110
1111111111	1023	1101111000100101

- How about 2K x 8bit? 16K x 10bit? 64K x 10bit?
- What is the relationship between the # of words and # of address bits?

Control Inputs to Memory Chip

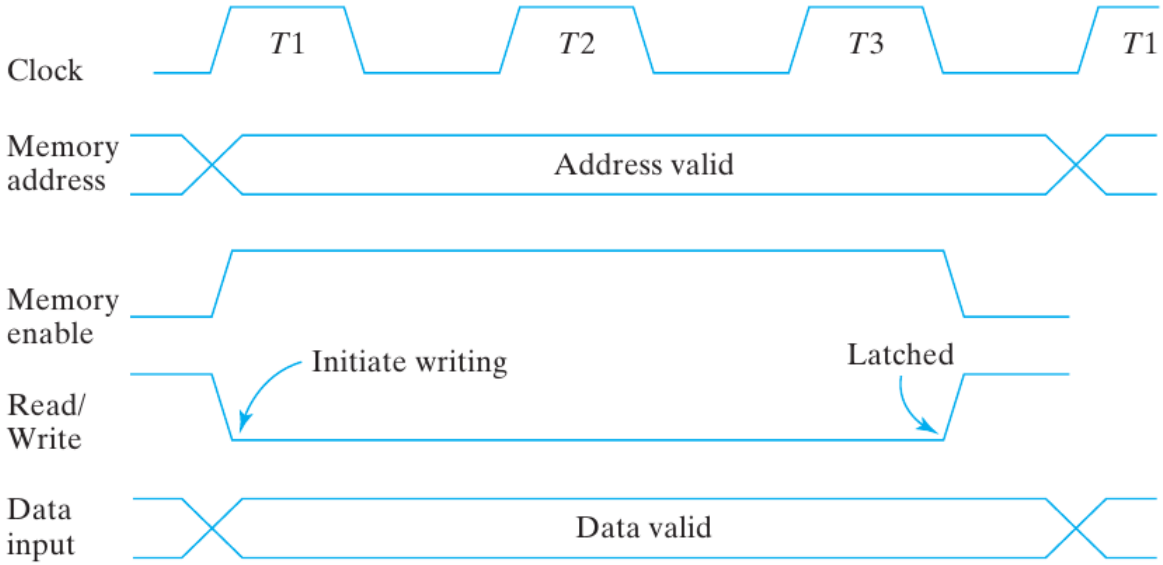
Table 7.1
Control Inputs to Memory Chip

Memory Enable	Read/Write	Memory Operation
0	X	None
1	0	Write to selected word
1	1	Read from selected word

Write Operation

1. Apply the binary addr. of the desired word to the addr. lines.
2. Apply the data bits that must be stored in memory to the data input lines.
3. Activate the write input.

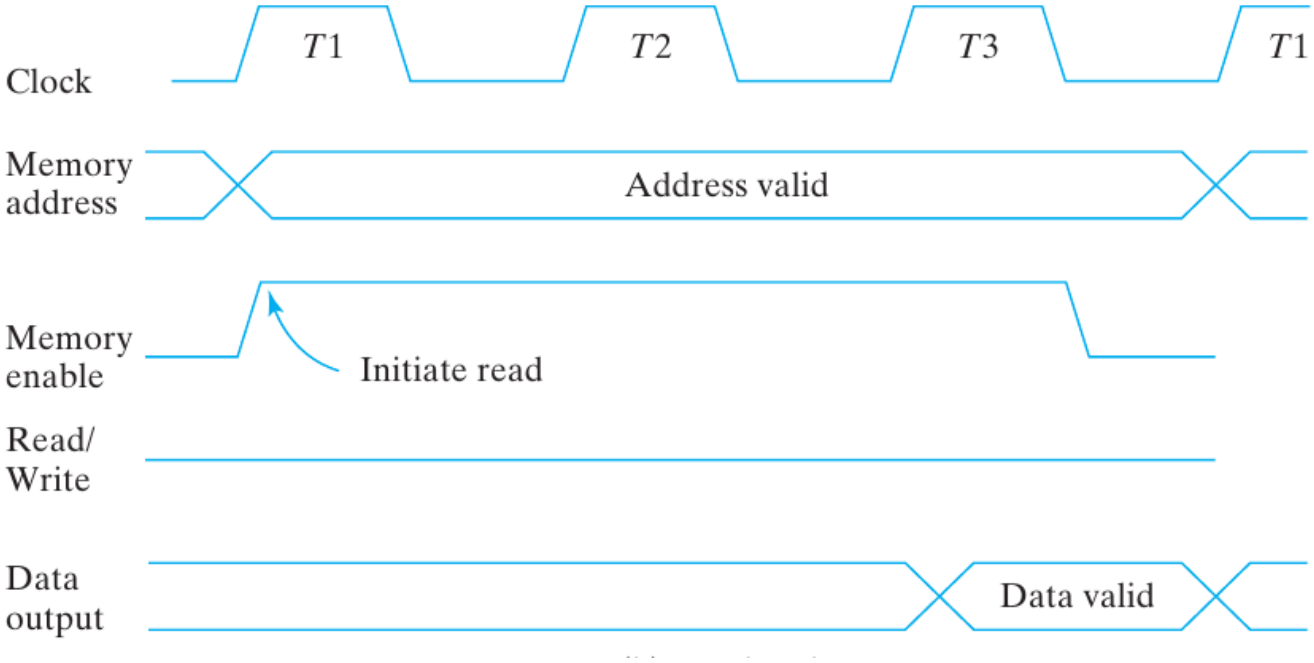
What is the access time?



Read Operation

1. Apply the binary address of the desired word to the address lines.
2. Activate the read input.

What is the access time?



Random Access Memory vs. Sequential Access Memory

- The mode of access of a memory system is determined by the type of components used.
- In a **random-access memory,** the word locations may be thought of as being separated in space, each word occupying one particular location. ➔ the access time is same
- In a **sequential-access memory**, the information stored in some medium is not immediately accessible, but available only at certain intervals of time. ➔ the access time is variable

Static RAM vs. Dynamic RAM

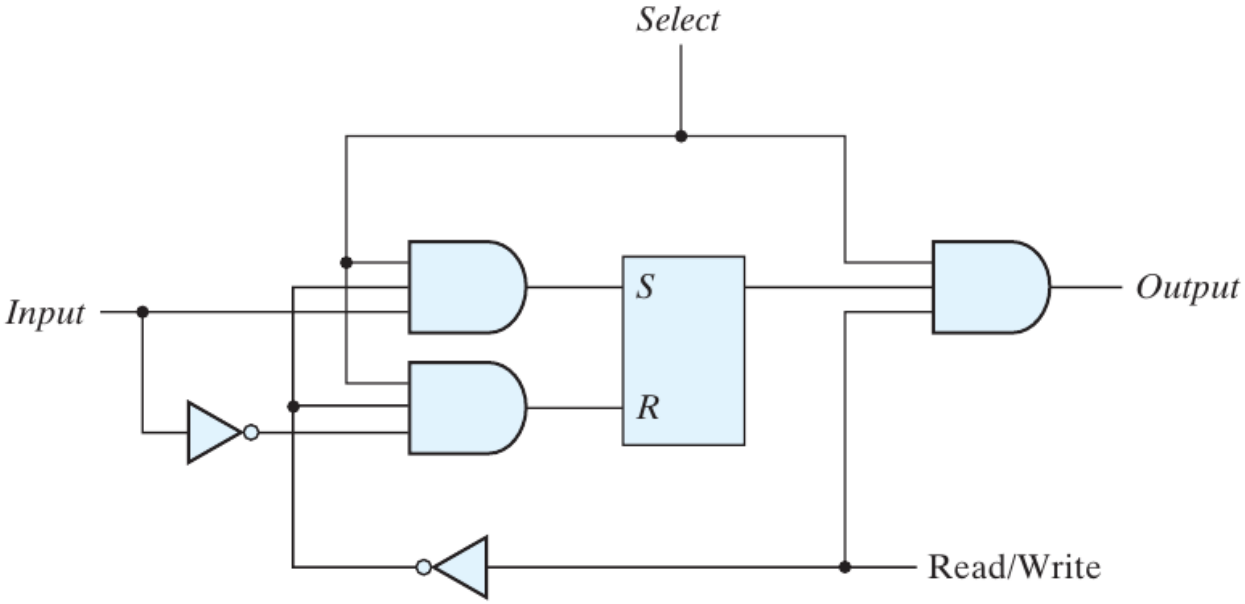
- Static RAM (SRAM) consists essentially of internal latches that store the binary information.
  - Stored data remains valid as long as power is applied to the unit.
- Dynamic RAM (DRAM) stores the binary information in the form of electric charges on capacitors provided inside the chip by MOS transistors.
  - The stored charge on the capacitors tends to discharge with time, and the capacitors must be periodically recharged by refreshing
  - Refreshing is done by cycling through the words every few milliseconds to restore the decaying charge.
- DRAM offers reduced power consumption and larger storage capacity in a single memory chip. SRAM is easier to use and has shorter read and write cycles.

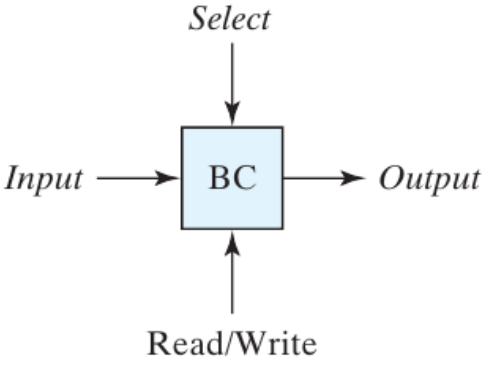
Volatile Memory vs. Nonvolatile Memory

- Volatile memory need external power to maintain the stored information.
- Nonvolatile memory, such as magnetic disk, retains its stored information after the removal of memory

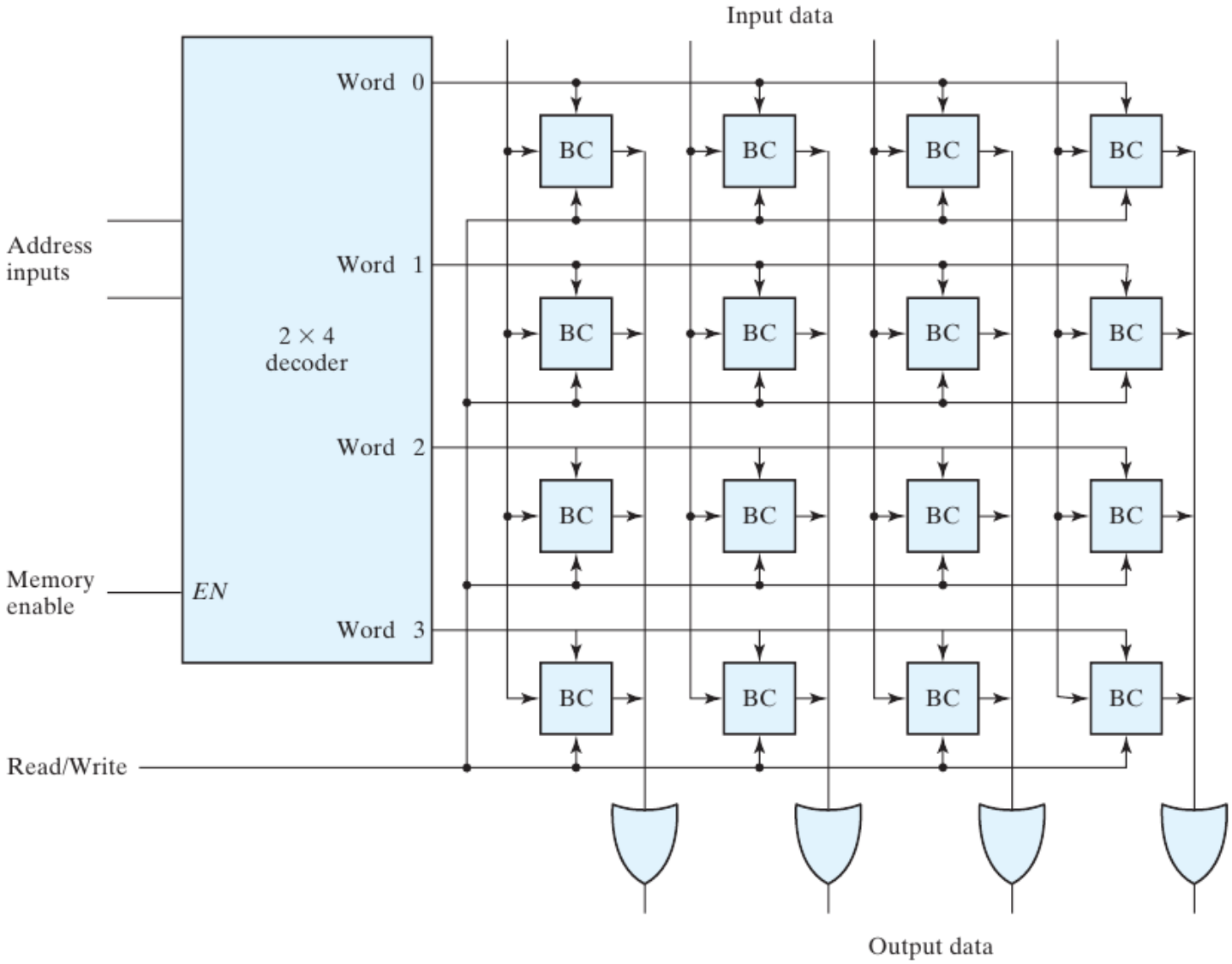
Procedure of Memory Access; Memory Bitcell Strcuture

- The internal construction of a RAM of m words and n bits per word consists of m × n binary storage cells.
- The equivalent logic of a binary cell that stores one bit of information shown below



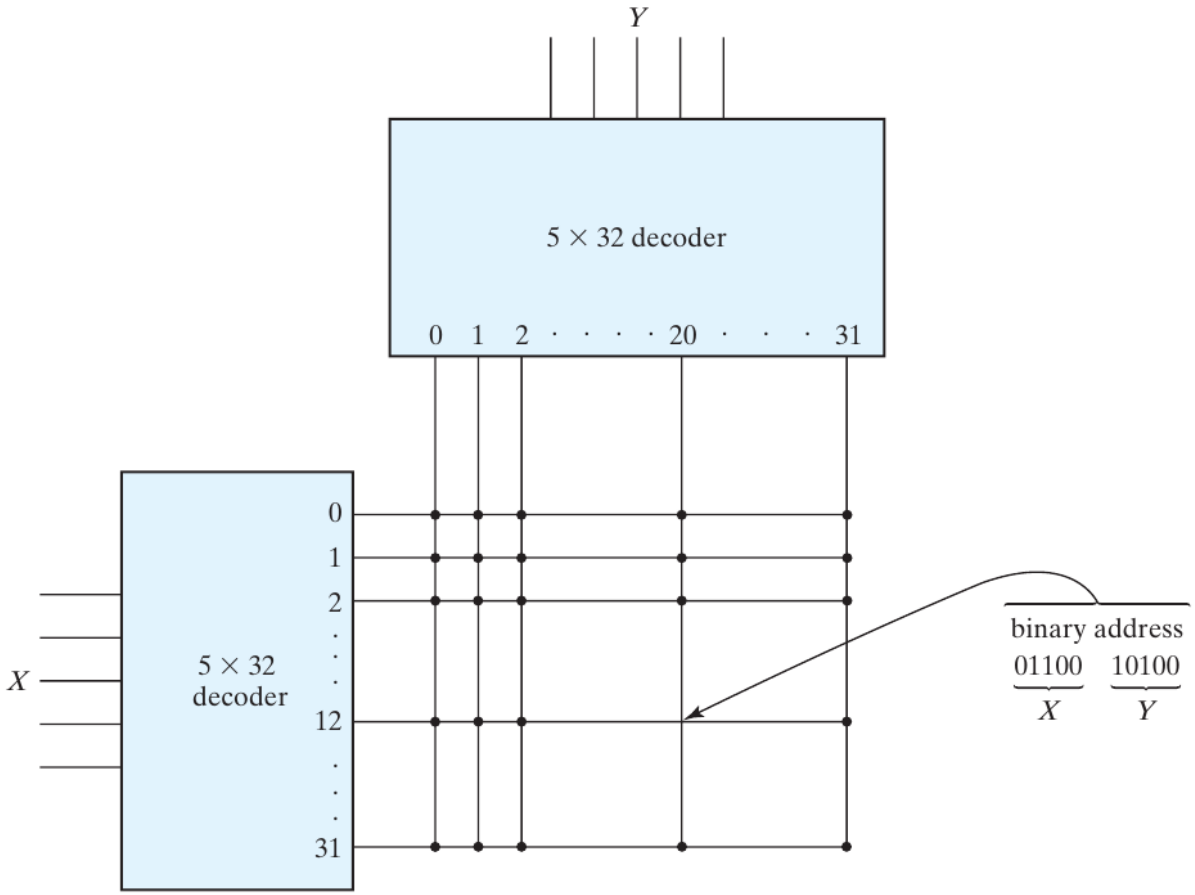


4x4 RAM


Input data
Word 0
Word 1
Word 2
Word 3
Address inputs
2 × 4 decoder
Memory enable
EN
Read/Write
BC
Output data

Coincident Decoding

- Instead of using a single 10 × 1,024 decoder, we use two 5 × 32 decoders.



Address Multiplexing for 64K DRAM

- A 2D array of cells arranged into 256 rows by 256 cols, for $2^8 \times 2^8 = 2^{16} = 64K$ words.
- Two address strobes
  - Row address strobe (RAS) enables the 8-bit row register.
  - Column address strobe (CAS) enables the 8-bit column register.

